CONDUCTIVE DIRECT BONDING OF IN-SITU DOPED POLYSILICON FOR MEMS WAFER-LEVEL PACKAGING

Vincent Pares[1,2], Amrid Amnache[1,2], Romain Stricher[1,2], Simon Landry[3], Paul Gond-Charton[3], Thierry Courcier[1,2], Serge Ecoffey[1,2], Luc G. Fréchette[1,2]

[1]Institut Interdisciplinaire d'Innovation Technologique (3IT); Université de Sherbrooke, Sherbrooke, QC, Canada
[2]Laboratoire Nanotechnologies et Nanosystèmes (LN2); CNRS IRL-3463, Université de Sherbrooke, Sherbrooke, QC, Canada
[3]Teledyne Dalsa Semiconducteur Inc. (TDSI), Bromont, QC, Canada

ABSTRACT

This paper presents the demonstration of conductive hydrophobic direct bonding between two In-Situ Doped Polysilicon (ISDP) films for MEMS wafer-level packaging. A key enabling factor for this direct bonding was the surface roughness reduction down to 0.22 nm RMS achieved using Chemical Mechanical Polishing (CMP) process, surpassing the minimal requirement. To evaluate the electrical characteristics of the bonded interface, daisy chain structures were realized, revealing low electrical resistance suitable for MEMS resonator applications. The average contact resistivity of 8 kΩμm^2, demonstrates superior electrical performances compared to other reported silicon/silicon interfaces. This opens the possibility of using polysilicon in bonded and conductive wafer-level packaging.

KEYWORDS

In-Situ Doped Polysilicon, Chemical Mechanical Polishing, Hydrophobic direct bonding, Contact resistivity

INTRODUCTION

Microelectromechanical systems (MEMS) devices are omnipresent in various industries, including automotive, consumer electronics, and healthcare. However, as these devices become more complex, the need for reliable and innovative packaging solutions has become increasingly important. Wafer-level packaging (WLP) offers advantages in terms of high-volume manufacturing, production yields and reduced fabrication costs. While various WLP bonding processes exist such as thermo-compression, eutectic, anodic, or silicon-to-oxide direct bonding [1], emerging devices introduce new integration challenges which limit the use of certain bonding technologies and the range of process parameters. For example, piezo-MEMS resonators require high thermal budget processes for packaging and the use of bonding films that can act as interconnexions, electrodes and vias which prevents the use of bonding technologies that do use metals [2].

Doped polysilicon is a promising candidate for bonding because of its low electrical resistivity and its ability to support temperatures above 1000°C. It is already used as an interconnexion material to fill through silicon vias (TSV) [3]. However, to perform high quality direct bonding and to extend the use of this material, the bonding surfaces require very low roughness, lower than 0.3 nm RMS [4]. As-deposited, low-pressure chemical vapor deposition (LPCVD) In-Situ Doped Polysilicon (ISDP) thin films result in rough surfaces of 2 to 5 nm RMS, preventing direct bonding. Chemical Mechanical Polishing (CMP) can be used to reduce this roughness, but the polycrystalline nature of the material still makes this challenging. The dopant segregation at grain boundaries modifies locally the effect of chemistry and consequently the polishing mechanism, while the different grains orientations result in anisotropic polishing rates [5].

The technological challenges associated to lower the roughness up to bondable level [6] have limited the study of polysilicon direct bonding application to mainly hydrophilic bonding with a requirement of 0.6 nm RMS [7]. Oxide free hydrophobic bonding is challenging with single-crystal Si and has never been demonstrated with ISDP.

This study aims to investigate the feasibility of using CMP to reduce the surface roughness of ISDP films and achieve high-quality conductive hydrophobic direct bonding for MEMS WLP. In particular, we focus on the use of bonded daisy chains as a way to characterize the contact resistivity of the bonded interface [8]. Electrical contact resistivity is benchmarked against values from literature.

METHODOLOGY

Contact resistivity

Fig. 1 shows a simplified schematic of bonded daisy chains and the equivalent resistance network for one contact. We can decompose the circuit (Fig. 1) in several resistance in series, with resistance from top and bottom ISDP lines (R_{top}, R_{bottom}) and resistance of ISDP related to intersection of bonded area ($R_{top-intersection}, R_{bottom-intersection}$) from which only the contact resistance is unknown.

The overall approach here is to compare the resistance measured for a significant number of contacts (R_m) and the resistance of the equivalent ISDP line without bonding interface ($R_{ø\ interface}$). The contact resistance contribution of the interface (R_c) is calculated according to eq. 1:

$$\boldsymbol{R_c = R_m - R_{\emptyset\ interface}} \qquad (1)$$

The contact resistivity ρ_c can then be calculated as:

$$\boldsymbol{\rho_c = R_c \times A_c} \qquad (2)$$

where A_c is the surface area for one contact between two films.

The daisy chains have several measurable lengths with up to 7300 contacts, with an area of 25 μm x 50 μm =1250 μm^2 each. The ISDP resistivity was measured on patterned ISDP lines (with a length of 500μm and width of 50μm) without contacts. All resistance measurements were carried out on Wentworth MP400, a probe station using four probes.

978-1-940470-05-4/HH2024/$25©2024TRF
DOI 10.31438/TRF.HH2024.111

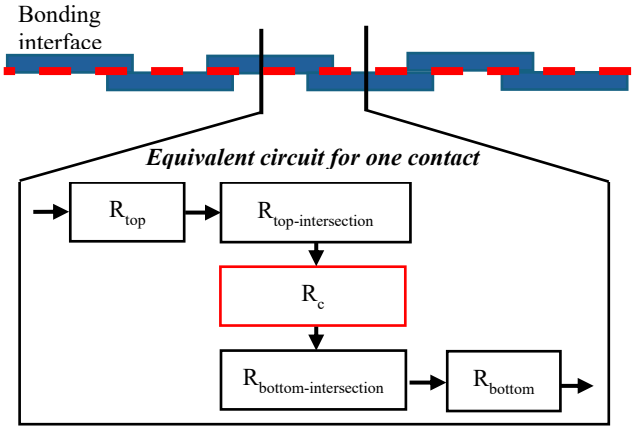

Figure 1: Cross-section schematic of bonded daisy chains and equivalent circuit with contact resistance of interface (in red)

Microfabrication process

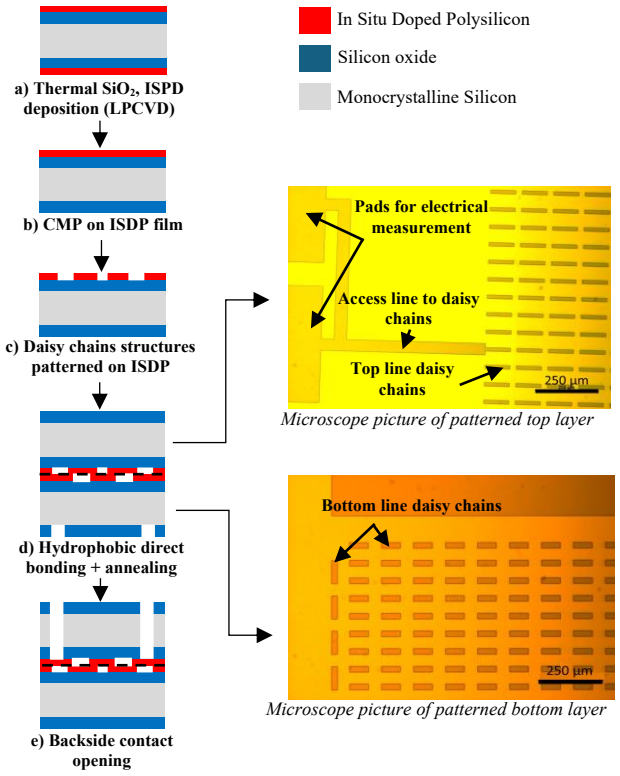

Figure 2: Process flow of ISDP-ISDP hydrophobic direct bonded daisy chains for electrical characterization

Figure 2 shows the microfabrication process flow for the fabrication of daisy chains using a wafer-level ISDP-ISDP hydrophobic direct bonding. A pair of 100 mm wafers and 750 µm of thickness are used. First, 330 nm of ISDP film is deposited by LPCVD on the top of 1.1 µm thermal SiO_2 (Fig.2a). This film is doped in situ with phosphorous concentration of 10^{20} atm.cm^{-3}. The bottom ISDP film is dry etched in order to allow the infrared post bonding visualization. A CMP process was developed specifically for this work to reduce surface roughness, ensuring compatibility with direct bonding requirements (Fig. 2b). A Alpsitec E460 CMP tool was used together with a Fujifilms commercial colloidal slurry (glanzox 3900) and suba600 polishing pad. The CMP process was developed by successive Design of Experiments to find a combination of parameters to be in the mixed lubrication regime. In this regime the chemical effect of slurry on silicon and mechanical forces applied allow targeted roughness reduction. In our case the most effective surface roughness reduction was obtained with an applied pressure equivalent to 300 g cm^{-2} with rotation speeds of polishing head of 70 rpm and 60 rpm for the pad. After CMP, the wafers were cleaned with room temperature SC1 1:1:5 followed by a mechanical scrubbing using PVA brushing system to remove particles and contamination, and dipped in a 1:50 diluted HF solution. Daisy chain structures were patterned in the ISDP films by plasma etching as illustrated in Fig.2c after CMP without significant impact of these additional microfabrication steps on surface roughness. Prior to bonding, the wafers were carefully cleaned with room temperature 1:1:5 SC1 solution for 15 minutes followed by a 60 second dip into diluted HF solution (1 HF: 50 H_2O) to prepare the surface for hydrophobic bonding. Dwell time between HF and bonding to limit the growth of native oxide was reduced to a minimum of 5 min. The two wafers were then bonded under vacuum at 400°C for 1 h with a uniform load of 5 kN (Fig. 2d). The bonded wafer pair was then annealed for 1 h at 1000°C in a nitrogen ambient. Reactive Ion Etching of SiO2 followed by Deep Reactive Ion Etching of 750 µm of Si was carried-out to reach the pads for electrical characterization (Fig. 2e). HF was used to remove the remaining SiO_2 on top of the electrical pads.

Surface characterization

Post CMP surface characterization was conducted using a Park System NX20 atomic force microscope (AFM). Measurements were taken after surface cleaning in 3 positions in the center, middle and edge of the wafer for uniformity assessment. This involved performing four scans in each position of 1 µm x 1 µm within a 2 µm x 2 µm square. The choice of this method to determine the global nano roughness of the surface is motivated by the polycrystalline nature of the surface and the need to have monitored many polysilicon grains, grain orientations and grain boundaries.

RESULTS AND DISCUSSION

CMP surface preparation

Figure 3a shows a surface AFM scan of as deposited ISDP highlighting a 3.4 nm RMS roughness and high peak-to-valley ratio numbers. Figure 3b shows the equivalent surface after CMP.

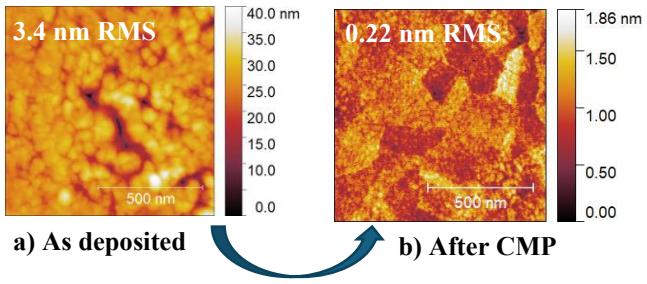

Figure 3: AFM scan of ISDP film as deposited (a) and after CMP (b)

It reveals grain boundaries and a 0.22 nm RMS roughness with low peak-to-valley ratio despite grains orientations. The AFM measurements across the wafer show a uniform surface roughness as long as a sufficient amount of ISDP is removed. For that specific film thickness and polycrystalline silicon, a minimum of 35 nm needs to be removed to reveal crystalized grains and remove the as deposited rough topography. Post-CMP surface cleaning did not impact the surface and no particular contaminations resulting from

CMP remain. After the cleaning steps, the RMS roughness varied less than 0,02 nm.

This CMP process using a commercial slurry demonstrated a defect free surface with RMS roughness of 0.22 ± 0.02 nm, which is below the target for hydrophobic direct bonding.

ISDP-ISDP direct bonding

Figure 4a shows a low-resolution infrared (IR) inspection of the bonded wafer pair. It reveals uniform bonding with limited local defects related to particle contamination. The bonding strength was evaluated using a blade insertion at the interface technique [9]. It was impossible to separate the wafers without breaking the Si, suggesting that bond strength is at least equal to or greater than the fracture energy of silicon.

Higher-resolution IR microscopy was used to zoom-in on the daisy chains as depicted in Figures 4b and 4c. No visual presence of contamination or defects at the interface, which could potentially impact the contact resistance, was observed. The bow of the wafer was measured with a profilometer before and after ISDP strip on one side. The bow increased from 4.5µm to 15µm, which is negligible in both cases and will not impact bonding. A bonding misalignment and rotation between the top and bottom wafer are measured and found to be: x = +6 µm, y = -10 µm, and θ < 1°. This misalignment was taken into consideration in the calculation of the contact resistivity.

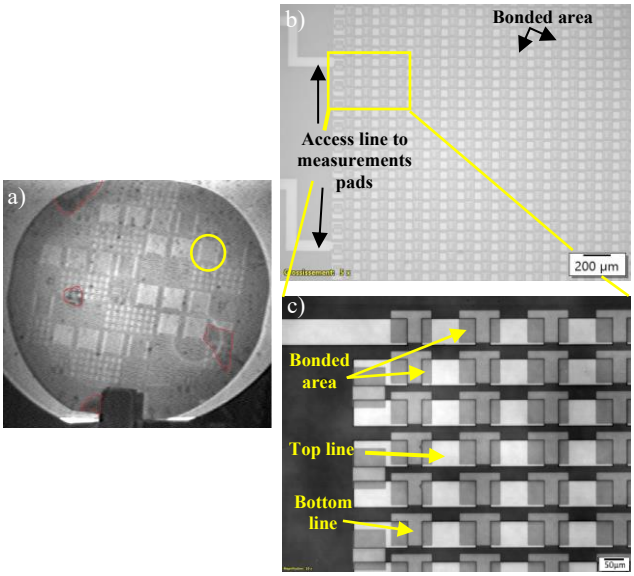

Figure 4: a) IR picture of the bonded interface (with bonding defect areas in red), b) IR microscopic picture of a part of a die with several contacts, c) zoom on contacts.

Contact resistivity

The ISDP bulk resistivity was measured before bonding and after the post-bonding anneal. The bulk resistivity decreased from 18.4 ± 0.3 Ωµm to 16.6 ± 1.1 Ω.µm, respectively. The electrical contact resistivity was then extracted from I-V measurements on daisy chains with numbers of contacts ranging from 2000 up to 7300 contacts. The calculation uncertainty mainly comes from thickness variation of the polished ISDP layer. Another source of error is the actual dimension of the structures due to variations between the designed and fabricated geometries. This error is minimized by measuring the actual dimensions.

Resistance measurements over the die did show ohmic behavior which confirms a good interface between the two ISDP surfaces. The uncertainty measurement associated to the four-point probe station must be considered, although in our case, given the sensitivity of the equipment and the I-V measured it is negligible.

By measuring the electrical resistance and calculating the resistance without interface, the electrical contact resistivity can be estimated from eq. 1 and eq. 2. The contact resistivities as a function of number of contacts are shown in Fig. 5. The average contact resistivity of hydrophobic direct bonding of ISDP films with associated standard error is 8,000 ± 2,500 Ω.µm².

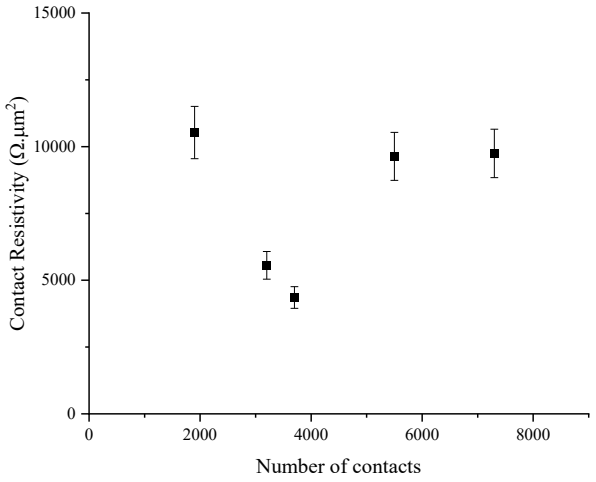

Figure 5: Extracted contact resistivity vs number of contacts

To our knowledge, there is no reference in the literature that did extract the contact resistivity of doped polySi/Si and Si/Si interfaces resulting from a bonding process. Figure 6 represents the measured resistivities of different types of Si-metal or Si-Si contacts from interfaces formed after the deposition (e.g., evaporation, LPCVD) of the second film on top of silicon, but not after a bonding process. All silicon materials reported in Figure 6 were doped with similar phosphorous concentrations, in the range of 10^{20} atm.cm^{-3}.

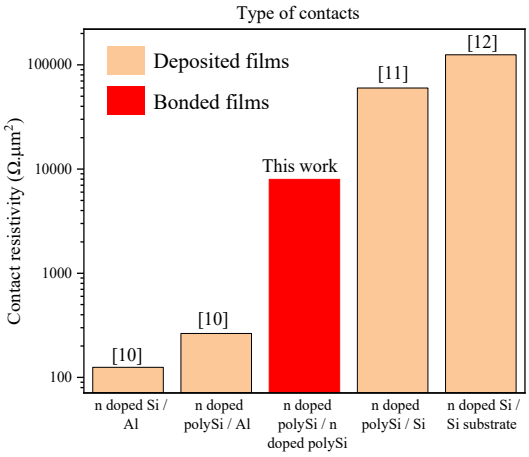

Figure 6: Si contact resistivity benchmark for different types of interfaces

Figure 6 shows that the contact resistivity extracted from the daisy chains is about 10 times lower than other reported silicon/silicon interfaces [11],[12]. Compared to other types of interfaces, encountered classically in MEMS industry and reported in literature such as metal/silicon interface, we are however two

orders of magnitude higher, as expected [10].

CONCLUSION

The demonstration and characterization of conductive hydrophobic direct bonding between two In-Situ Doped Polysilicon (ISDP) films showed promising performance for MEMS WLP technology. Roughness reduction of ISDP films by development of a chemical mechanical polishing process achieving a remarkable surface roughness of 0.22 nm RMS enabled this bonding. Through daisy chain structure characterization, we extracted an average contact resistivity of 8,000 Ω.µm², demonstrating promising performance compared to other reported silicon/silicon interfaces. This bonding interface exhibits negligibly low electrical resistance suitable for resonator MEMS applications. This work therefore opens the possibility of using polysilicon as an electrical contact as well as bonding interface for WLP MEMS, including devices requiring high temperatures processing, such as high Q resonators and gyroscopes.

ACKNOWLEDGEMENTS

The author would like to acknowledge the support from the Canada Research Chair Program (NSERC), PROMPT, Teledyne DALSA and CMC through MNT financial assistance.

REFERENCES

[1] Liu, P., Wang, J., Tong, L., and Tao, Y. (April 29, 2014). "Advances in the Fabrication Processes and Applications of Wafer Level Packaging." ASME. J. *Electron. Packag*. June (2014)

[2] G. Pillai and S. -S. Li, "Piezoelectric MEMS Resonators: A Review," in *IEEE Sensors Journal*, 1 June (2021) vol. 21, no. 11, pp. 12589-12605

[3] Dixit, Pradeep; Vehmas, Tapani; Vähänen, Sami; Monnoyer, Philippe; Henttinen, Kimmo. ``Fabrication and electrical characterization of high aspect ratio poly-silicon filled through-silicon vias.`` *Journal of Micromechanics and Microengineering*, (2012)

[4] H. Moriceau; F. Rieutord; F. Fournel; L. Di Cioccio; C. Moulet; L. Libralesso; P. Gueguen; R. Taibi; C. Deguet ``Low temperature direct bonding: An attractive technique for heterostructures build-up``. (2012), 52(2), 331–341.

[5] Forsberg, M & Keskitalo, Niclas & Olsson, Jörgen. ``Effect of dopants on chemical mechanical polishing of silicon``. *Microelectronic Engineering*. (2002). 60. 149-155.

[6] Stricher, R., Gond-Charton, P., Amnache, A., Campos, J. F. A., Frechette, L., Drouin, D., & Ecoffey, S. ``In Situ Doped Polysilicon (ISDP) Hydrophilic Direct Wafer Bonding for MEMS Applications``. *ECS Journal of Solid State Science and Technology*, (2021).

[7] Romain Feilleux. ''Polycristalline silicon direct bonding mechanism.'' Micro and nanotechnologies / Microelectronic. University of Grenoble, (2011)

[8] Beilliard, Yann & Coudrain, Perceval & Cioccio, Léa & Moreau, Stephane & Sanchez, Lesly & Montmayeul, Brigitte & Signamarcheix, Thomas & Estevez, Rafael & Parry, Guillaume. ``Chip to wafer copper direct bonding electrical characterization and thermal cycling``. (2013)

[9] Q.Y. Tong, U. Gosele,"SemiConductor Wafer Bonding: Science and Technology", John Wiley Sons Inc (1998)

[10] Naguib, H. M. "AL/Si and Al/Poly-Si Contact Resistance in Integrated Circuits." *Journal of The Electrochemical Society*, (1977)

[11] Rienacker, Michael; Bossmeyer, Marcel; Merkle, Agnes; Romer, Udo; Haase, Felix; Krugener, Jan; Brendel, Rolf; Peibst, Robby. ``Junction Resistivity of Carrier-Selective Polysilicon on Oxide Junctions and Its Impact on Solar Cell Performance``. *IEEE Journal of Photovoltaics*, (2016), 1–8.

[12] Li, Y., Van Toan, N., Wang, Z. et al. Formation and Evaluation of Silicon Substrate with Highly-Doped Porous Si Layers Formed by Metal-Assisted Chemical Etching. *Nanoscale Res Lett* 16, (2021), 64.

CONTACT

*Vincent Pares, tel : +1-819-919-2442 ;
vincent.pares@usherbrooke.ca