AN SOI-PCB WITH THERMOCOMPRESSION BONDED CMOS, MULTILAYER WIRING, AND NATIVE MEMS

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ABSTRACT

In this paper, we introduce a silicon-on-insulator (SOI) platform that integrates MEMS and foundry-fabricated CMOS integrated circuits through a thermocompression bonding (TCB) process. This compact design features chip-level integration with a ≤ 5 µm pitch and multilayer electrical connectivity. The electrical interface comprises a three-layer metal stack — Chromium, Platinum, and Gold — deposited on polysilicon and silicon nitride insulation layers. The device employs a two-layer wiring scheme enabled by Au-Au TCB. We assess the bonding strength and electrical properties, including the resistance of metal traces, interlayer vias, and MEMS contacts on two 2×2 cm^2 SOI-PCB chiplets. Further, we perform heterogeneous integration between the foundry-fabricated CMOS and the SOI-PCB, utilizing TCB for the interface between CMOS copper bumping and gold traces. We conduct comprehensive tests of electrical connectivity, power characterization, and demonstrate chip bring-up conducted across the SOI-PCB interface.

KEYWORDS

Thermocompression bonding (TCB), MEMS CMOS Integration, Silicon Interconnect Fabric (Si-IF)

INTRODUCTION

Interest in integrating CMOS and MEMS devices is growing due to the demand for more compact and capable sensor motes and micro robotic systems with integrated sensing, actuation, and computing capabilities. Heterogeneous integration of CMOS chiplets with MEMS devices bridges the gap between ICs fabricated in advanced nodes and MEMS devices produced through non-standard microelectronics fabrication methods. This integration can minimize device interference factors such as thermal budgets, chemical compatibility, and metallization [1]. Previous work by Gomez, et. al. employed a zero-insertion force (ZIF) socket with spring-loaded contacts to interface MEMS devices with CMOS ICs in complex 3D micro-assemblies [2]. Compared to this method, the integration strategy we show in this work simplifies heterogenous CMOS-MEMS integration by utilizing thermocompression bonding (TCB) at the die-to-die interfaces, while also enabling the design of 3D micro-assemblies in the SOI platform itself.

Solderless metal TCB is a well-established method for interfacing noble metals like gold (Au-Au) at the wafer level [3]. Researchers have reported success in forming intermetallic compounds such as Au-Cu [4] and Au-Al [5] through metal compression bonding, by addressing challenges related to oxide removal at the interface. The concept of CMOS-MEMS integration using flip-chip style contact bonding has been validated in commercially available devices [6]. However, these packaging solutions primarily focus on providing limited external electrical contacts to MEMS devices and utilize only a single metal routing layer. This limitation constrains the construction of more advanced routing necessary to integrate modern ICs. In this work, we aim to address both the quality of the TCB metal interface and the capability for multi-layer tracing with our innovative SOI-PCB device.

FABRICATION

Device Preparation

The SOI-PCB fabrication involves a three-mask process on two different SOI wafers. Stoichiometric silicon nitride and polysilicon layers are deposited onto the bare SOI wafers, serving as the insulator and the structural body of the insulated electrical layer, respectively. These bilayers are then patterned and etched to isolate traces from the device layer. A lift-off process provides the patterning of the evaporated Cr/Pt/Au stack, with thicknesses of 10 nm, 10 nm, and 650 nm, respectively, to form conductive traces, silicon MEMS contacts, and interlayer vias. This process achieves feature sizes as small as 2 µm. Platinum is strategically placed between chromium and gold as a diffusion barrier and is essential for the bonding processes. Silicon MEMS devices are crafted on the 40 µm thick single-crystal silicon layer using deep reactive-ion etching (DRIE), like fabrication method described in [7]. The same fabrication steps are replicated on both SOI wafers, albeit using different masks.

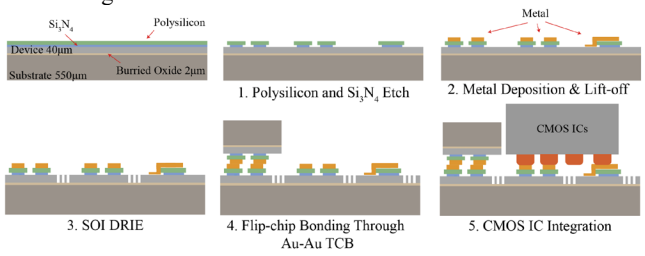

Figure 1. Fabrication process steps and final cross-sectional view of the presented SOI-PCB and CMOS IC showing four independent electrically conductive layers, MEMS structures embedded in the SOI layer, and electrical contacts between the insulated electrical layer and MEMS.

Wafer Level Gold-to-Gold Bonding and Device Release

Each SOI wafer, complete with a patterned device layer and insulated metal layer, forms half of the final device structure. These wafers are aligned and joined through an Au-Au thermocompression bonding process at the gold pads. This procedure also establishes interlayer vias between the insulated electrical layers via the same bonding pads. Prior to bonding, test chips are preconditioned with O_2 plasma. The strength of the Au-Au thermocompression bonding (TCB) increases linearly with the bonding temperature and pressure, with an optimal bonding temperature identified at 325 ℃ and a tool temperature at 300 ℃ to balance device integrity and bonding efficacy [8]. The detailed experimental conditions for the Au-Au thermal compression bond are listed in Table 1.

Table 1: Au-Au Bonding Conditions

Process	Conditions
Surface Preconditioning by RF plasma	O_2: Equivalent to ~140 A/min PR Removal Rate
Bonding	500 N (load), 325 ℃ (base), 300 ℃ (top plate), 1 hour, 5×10^{-6} Pa (chamber)

CMOS-MEMS Heterogeneous Integration

Post-device release, gold bonding pads on the SOI-PCB, which

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interface with the CMOS ICs, become accessible. We interface the SOI-PCB with a custom system on chip (SoC) fabricated using the Intel-16 process with Cu bumping for flip-chip packaging. The Cu bumps are approximately 20 µm in height and 80 µm in diameter, arranged with a 130 µm pitch. The main challenge in establishing reliable Cu-Au thermocompression bonding is managing the copper oxidation at the interface. Sahoo et al. have shown successful gold-to-copper thermal compression bonding after copper oxide removal through formic acid treatment. However, since such chemicals are less commonly used in standard foundry processes and custom bonding tool, we propose an alternative surface preparation method that utilizes ion milling. Argon ions generated at 1×10^{-4} Torr gently clean the SoC surface for 2 mins. Following this preparation, copper bumps on the CMOS ICs are aligned and bonded to the gold contacts using a Finetech FINEPLACER 96 Lambda flip-chip bonder, under an environment of 10% hydrogen forming gas at 300 ℃ platen temperature with 10 N force applied. The temperature and load are selected to maximize the adhesion between gold and copper while minimizing the likelihood of damaging the SoC.

Table 2: Au-Cu Bonding Conditions

Process	Conditions
Cu bumping Surface activation by RF plasma	Ar, Chamber pressure, $5\times 10^{-6}\ Pa$, $500V$ (beam voltage), $200mA$ (beam current)
Au surface preconditioning by RF plasma	O_2: Equivalent to $\sim 140A/min$ PR Removal Rate
Bonding	10 N (load), 325 ℃ (base), 300 ℃ (top plate), 500s

MECHANICAL TESTING

Au-Au Thermocompression Bonding

Cr/Au thin film is a well-documented process for lift-off metal deposition. The bilayer thin film is popular for its high corrosion resistance and low electrical resistivity in MEMS applications. However, this thin film is not an ideal material selection for TCB process as Cr diffuses to Au surface and forms oxidized islands that prevent proper contact during TCB. [9]. Instead, we use Pt as a diffusion barrier between Cr and Au to improve the surface quality of Au bonding interfaces while preserving Cr as a corrosion resistant adhesion layer. However, a Pt diffusion barrier reduces the adhesion strength of the film by preventing the formation of Cr-Au alloy. Mechanical performance test chips with 10 nm Pt diffusion barrier are shown in Figure 2.

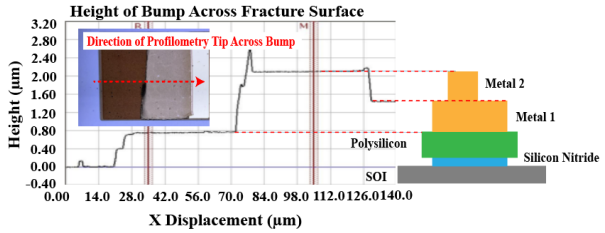

Figure 2. Microscope image of an Au-Au bond site across a fracture site with both cohesive and adhesive failure with its corresponding height measured in profilometry and cross section view. The direction of the profilometry scan is indicated by the red arrow.

Test chips featuring arrays of 10×10 µm^2 contact pads undergo tensile and shear test. An ultimate tensile strength of 13.9 MPa, and an ultimate shear strength of 20.4 MPa is observed. SEM image of the fracture site suggests delamination occurs along between polysilicon and silicon nitride interfaces. This implies that a proper adhesion between the Au-Au interface, with no Cr observed on the surface.

Au-Cu Thermocompression Bonding

We evaluate two designs of Au contacts: a square contact pad of 60×60 µm and a donut-shaped Au contacts with dimension of 80 µm (outer diameter) $\times$ 45 µm (inner diameter) as shown in Figure 3. Au contacts are designed to be smaller than the copper bumping on SoC in both cases, so the copper bumping can deform and wrap around the gold for a stronger bond. Figures X, Y, and Z show the fracture sites after the bonded CMOS ICs are removed. Fragments of Au contact pads adhere to copper bump of the SoC and expose the underlined silicon nitride. The delamination between poly-Si and silicon nitride indicates strong adhesion between Au-Cu interface. The fracture site for square contact is approximately 2×10^3 µm^2 versus 1.7×10^3 µm^2 for looped contact pads, which reflects higher bonding strength in square contacts.

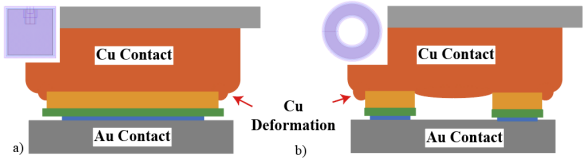

Figure 3. a): Design of rectangular Au contact pad for Cu bumping (upper left) and its cross-section illustrated b) Design of donut-shape Au contact pad (upper left) and its cross-section interface.

We also observed lumped circular-shaped copper residue adhering to the SOI device layer outside of the bonding region as far as 10 µm apart from the edge of metal layer, shown in Figure 4. The copper bumps deform by more than 1.3 µm and wrap around the gold contact pads and agglomerate on the device layer during the TCB process. This defect is observed in both contact pad designs and would create a low impedance path between contacts through the silicon device layer. Therefore, a larger, ~80 μm in diameter, circular gold contact pad is preferable to interface with CMOS copper bumping.

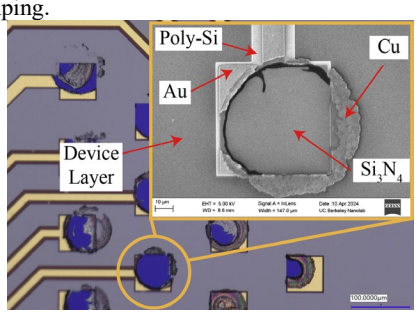

Figure 4. SEM image of rectangular Au contact pad after SoC removal. EDX measurement verifies that Cu deforms and fractures near the edge of contact pads and deposits on the SOI device layer. The Au contact pad at the center delaminates on the poly-Si and silicon nitride interface.

Across the die, all Au contact pads show signs of fracture after CMOS chip removal, suggesting 100% bonding yield. The bond strength uniformity evaluated with the degree of fracture across the 2×2 mm bonding site is shown in Figure 5. Large metal and poly-Si delamination are concentrated near the right edge of the chip indicating a strong adhesion. The contact pads marked in

yellow showed only metal fracture after debonding, with 50% of the overall pad metal removed. The contact pads with partial damage are concentrated in the center of the bond site. The copper bumps remained mechanically connected to the Au contact pads in the partially damaged regions. The nonuniformity in bonding strength travels from right to left of the bonding site. This error is likely caused by the angle variation as the SoC chip is brought into contact with SOI-PCB on the flip-chip bonder.

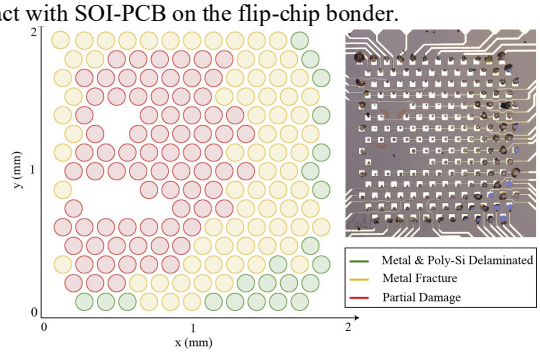

Figure 5. Visual inspection of Au contact pads after removing the SoC. Figure of merit on bond quality is assigned to different degree of damage to the contact pads. Bond of the 2×2 *mm SoC results in* 100% *bonding yield.*

ELECTRICAL TESTING

SOI-PCB Characterization

A test structure was fabricated to characterize the resistivity of the SOI-PCB's insulated electrical layer, shown in Figure 6. The electrical layer exhibited a linear current-voltage characteristic, affirming Ohmic contact over the nitride step. Resistance decreased from 5.88 Ω to 5.05 Ω over nitride steps and 3.43 Ω to 2.68 Ω within the electrical layer as the trace width increased from 10 to 140 µm over a 350 µm length. Resistance over interlayer via is 0.52 Ω for 10×10 µm contacts.

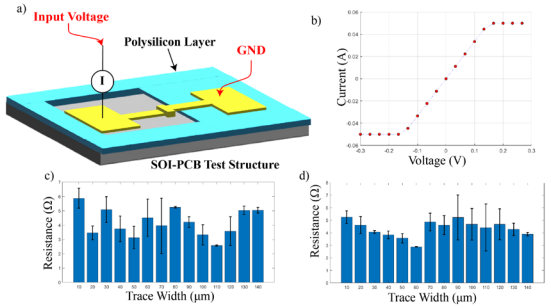

Figure 6. a): Configuration of the electrical test for resistance on a trace from SOI layer to the insulated electrical layer over a nitride step. b) I-V characteristic of a 350 *µm long,* 10 *µm wide trace over the nitride step. c, d) Mean resistance measurement of trace with width between* 10 *µm to* 140 *µm over a nitride step (left) and in insulated electrical layer (right)*

CMOS Power Test

We use SCµM-V, a custom crystal-free SoC for IoT applications, as the CMOS IC for integration with the SOI-PCB. SCµM-V is designed in the Intel 16 FinFET process and provides validation that the SOI-PCB is suitable for integration of ICs fabricated in advanced process nodes. A description of a newer generation of the SCµM-V SoC will be provided in [10].

An initial proof-of-concept is demonstrated by characterizing the CMOS SoC's on-chip power management system following thermocompression bonding to the SOI-PCB. The SOI-PCB is then wire bonded from contact pads to a custom breakout PCB. This breakout PCB serves as an adapter between the SOI-PCB and standard-pitch headers for ease-of-test, depicted in Figure 7. Power is supplied through 1.5 V and GND connections at two SOI-PCB gold contacts as shown in Figure 8. On-chip bandgap reference voltage is measured at 1.13 V, exceeding the expected circuit behavior; we attribute this to contact with a neighboring LDO regulator output bump due to the copper deformation discussed in the previous section. Next, the SoC's RISC-V 32-bit microprocessor is supplied with 0.85 V through a TCB contact, and a static current consumption of 39.9 mA is measured. This current consumption matches corresponding measurements taken of the SoC during bring-up characterization that used traditional flip-chip packaging methods. Lastly, the Cu/Au contact resistance is also approximated by measuring the resistance between two adjacent GND pins from the PCB. We approximate a resistance value of 2 Ω per contact.

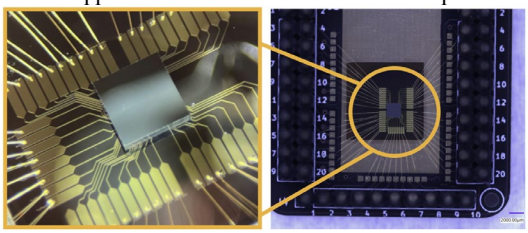

Figure 7. Microscope view of the SOI-PCB and CMOS SoC after bonding (left). The assembly is connected to a regular PCB through Au wire for functionality tests (right).

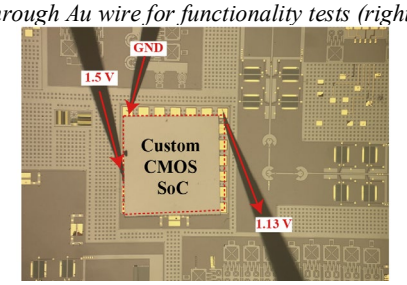

Figure 8. Configuration of the electrical test for bandgap readout of the CMOS SoC with copper bumping through gold contact on SOI-PCB with MEMS device in SOI before release.

CMOS Bring-up Test

The same SoC is also connected in the configuration described by Figure 9. SoC basic functions, such as the external boot bus initialization and on-chip clock generation and distribution, are tested. Three voltage domains are supplied through the SOI-PCB to power the digital core (0.85 V), the analog clock generator (1 V), and the IO level-shifters and pad drivers (1.8 V). The analog and IO current consumption through the SOI-PCB – 3 mA and 357 μA, respectively – match measurements taken with traditional packaging and PCB bring-up methods.

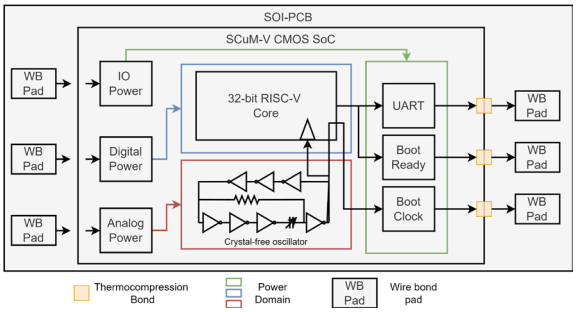

Figure 9. Diagram of the SOI-PCB and CMOS SoC connections for the bring-up test. Three power domains are supplied and three

indicators of the SoC's boot status are broken out through TCBs at the die-to-die interface.

After power-up, the SoC's UART transmit and "boot ready" signals measure 1.79 V, indicating that IO level shifters and pad drivers are powered. The SoC has several on-chip, crystal-free oscillators, one of which generates a clock with a frequency from 23 MHz to 40 MHz. At startup, the latter, lower frequency clock, is distributed to the 32-bit RISC-V core as the boot clock. In the digital domain, this clock is buffered by an IO pad driver as part of the off-chip tethered boot bus. This buffered output clock is then measured after the SOI-PCB to validate the SoC's startup conditions. Measurements of this signal, taken at the breakout PCB header, show a 28 MHz, 1.8V peak amplitude clock. The SoC's clock waveform, shown in Figure 10, has both frequency and amplitude within the expected startup bounds. The minimum voltage of the clock signal measured -0.32 V, likely due to poor calibration and a low-quality ground reference connection.

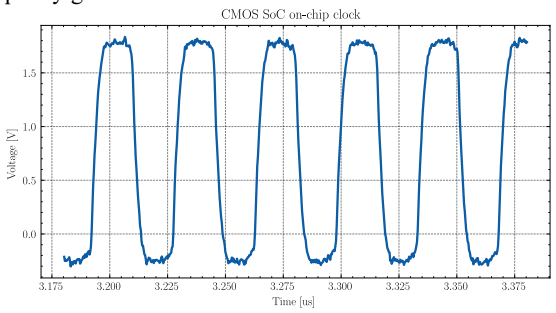

Figure 10. The waveform of the on-chip clock as measured after wire bonding from the SOI-PCB to the test PCB. The mean frequency of the clock is 28.2 MHz with peak voltages at 1.84 V and -0.32 V.

FUTURE WORK

In the future, we aim to introduce a second MEMS device layer to the top SOI wafer introduced in step 4 of the fabrication flow. The second device layer allows design of 3D MEMS devices such as out-of-plane hinges and rotary mechanisms. Release of the top device layer involves removal of the top substrate, reducing the size and weight of the final device. This evolution of the fabrication process will require deposition of parylene to protect the device layers of the bonded SOI wafers during substrate silicon removal in KOH. The device is then released in vapor HF before CMOS integration. The final device cross section is shown in Figure 11.

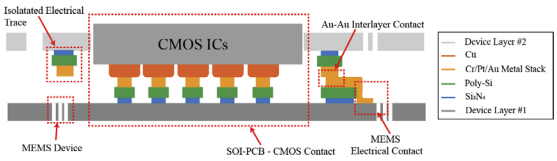

Figure 11. Cross-sectional view of future device with two SOI device layer and substrates removed for thinner and lighter packaging.

CONCLUSION

We introduce an innovative approach for embedding CMOS chips onto native MEMS processes with multilayer electrical connectivity without additional conductive adhesive. The achieved bonding accuracy and mechanical strength, along with the demonstrated electrical performance, underscore the feasibility and robustness of this TCB Si-IF process. These results provide a unique path to heterogenous CMOS-MEMS integration, enabling many applications such as on-silicon CMOS control of MEMS actuators, and sensors without wire bonding. This work paves the way for advanced heterogeneously integrated systems, promising improved compactness, efficiency, and versatility within simpler packaging processes.

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