WAFER-LEVEL HIGH-ASPECT-RATIO DEEP REACTIVE ION ETCHING OF 4H-SILICON CARBIDE ON INSULATOR SUBSTRATES

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ABSTRACT

This paper reports on the results of high-aspect-ratio (HAR) Deep Reactive Ion Etching (DRIE) of thick 4H-SiC on Insulator (SiCOI) substrates at wafer-level and outlines the progress and challenges. Different size vertical trenches with high aspect-ratios of 15:1 ~ 20:1 and smooth sidewalls were achieved using electroplated nickel mask on 100mm SiC wafer, and a trench depth uniformity of 2% (±1μm) was measured across the wafer. The transferred recipe on SiCOI substrate was able to reach the buried oxide on all corners of the patterned SiCOI area while it created footing less than 100nm. The trench taper angle was 88.5º with a smooth sidewall, roughness < 120nm, resulting in 4H-SiC bulk acoustic wave resonators with Qs > 2M. These HAR DRIE results at wafer-level are a promising step to enable volume-manufacturing of ultra-high Q SiC resonators, which was previously done at die/small piece level.

KEYWORDS

SiC, SiCOI, DRIE, high-aspect-ratio, ultra-high Q, BAW

INTRODUCTION

Micromechanical resonators have several applications in consumer electronics, robotics, wearable sensors, and inertial navigation. Resonance quality factor is a key performance metric to evaluate the robustness of these micro-electromechanical devices. Although silicon is a well-established material for high-Q resonator applications, monocrystalline SiC promises much smaller intrinsic phononic loss for ultra-high Q applications, potentially 30x smaller than silicon counterparts [1]. Bonded monocrystalline SiCOI substrates allow MEMS device manufacture by providing a layer for release, and are a promising platform for the implementation of ultra-high Q resonators and coriolis gyroscopes owing to SiC's exceptionally high Akhiezer limit ($f \cdot Q = 6e14\ Hz$) [2].

Silicon carbide is a difficult-to-etch material, and HAR etching of SiC [3-6] is a dirty process due to requiring a hard metal mask such as nickel. The high-aspect-ratio etching of SiC is even more difficult due to the non-volatile etch by-product, i.e. NiC_xF_y, that alters the trench profile by blocking the trench opening, and changes the chamber condition by depositing on the etch chamber sidewall [1, 7]. The passivation growth causes major drift in the trench profile and sidewall surface roughness.

The lack of suitable high-density plasma etching tools with reasonable Mean Time Between Cleans (MTBC) of 100~130 hours at universities, along with the high cost of SiC wafers have hindered the development of HAR DRIE of SiC at wafer level. In addition to the challenge of precisely micromachining SiC [3, 8, 9], other barriers inhibiting the development of SiC MEMS include high material cost and difficult and time-consuming fabrication processes to manufacture SiC-on-Insulator (SiCOI) substrates. The sum of above-mentioned challenges makes the wafer-level implementation and study of thick 4H-SiC capacitive devices challenging and expensive. This paper reports on the progress that has been made in the HAR DRIE of 4H-SiCOI substrate at wafer level using industrial high-density plasma etching tools.

MATERIAL AND METHODS FOR HAR DRIE OF 4H-SIC-ON-INSULATOR

We fabricated 100mm 4H-SiCOI substrates by bonding SiC wafers to silicon handle wafers using SiO_2 TEOS as an intermediate bonding layer, followed by grinding and polishing. The buried oxide thickness was ~3μm and the targeted device layer thickness was 40μm. Several SiC and SiCOI wafers were coated with Cr/Au seed layers, patterned with AZ 9260 PR and nickel electroplated for ~6.5μm, Figure 2. The CD size for the device fabrication at wafer level was 3.5μm, although the nickel mask on these wafers included openings with several dimensions to study the DRIE lagging effect. To preserve samples and reduce development cost, the HAR DRIE recipe development plan included multi-stage transition from bulk SiC wafer piece to SiCOI wafer piece followed by a bulk SiC whole wafer and finally, transferring the recipe to SiCOI whole wafer. The 4H-SiC HAR DRIE recipe was developed at SPTS Technologies, using a Synapse™ module, Figure 2. The Synapse™ uses a doughnut shaped RF source to produce a high-density plasma for the etching of strongly bonded materials such as SiC, with improved mean time between cleans. The details of a typical baseline SiC DRIE recipe are presented elsewhere [10].

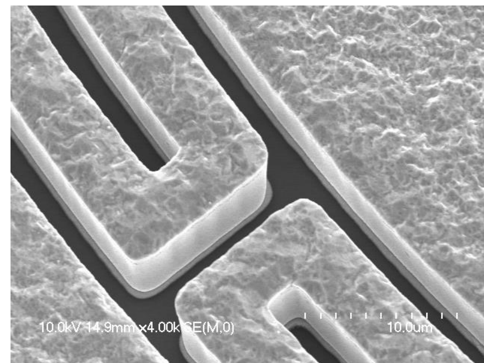

Figure 1: SEM of electroplated nickel mask (6.5 μm). The remaining seed layer on the substrate at the border of Ni mask reveals the sidewall are not completely vertical.

The requirements for the HAR DRIE etching of a 3.5μm CD trench feature in SiC focussed on achieving the 45μm target depth to reach the oxide stop layer while avoiding damage from the process, such as sidewall roughness and notching. To achieve this, development was started in the SPTS Synapse™ module by etching the target feature with a process typically used for 50μm CD through-wafer-via applications. The key modifications to this process that allow clean etching of the trench features were the reduction of pressure, reduction of platen power, and increased gas flows. The alterations to gas flows and platen power increased the etch rate of the feature. In the case of the gas, this allows more chemical etching of the SiC, and for the platen power it is suggested that reduced platen power limits the sputtering of the Ni

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mask into the feature opening. Transfer of the process to SiCOI wafers was completed to the target depth, with low sidewall roughness and minimal notching on the oxide layer.

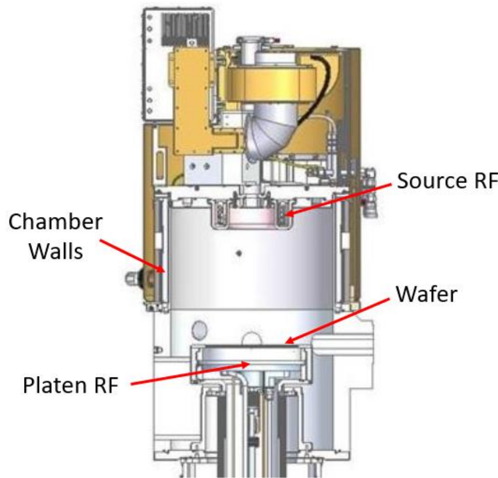

Figure 2: Schematic of the SPTS Technologies Synapse™ module

EXPERIMENT RESULTS

As mentioned above, different mask openings were present in the test pattern to investigate the effect of the mask opening on the etch depth achievable in a fixed time, in this case 65 minutes. The results are summarized in Figure 3. Figure 4 depicts the optical image of the first whole SiCOI wafer etched after the multi-stage recipe transfer from SiC and SiCOI wafer pieces to whole wafers. The cross-sectional SEMs of Figure 5 show the electroplated nickel mask is not vertical at the very top, causing some seed layer to remain due to shadowing effect. However, this has minimal effect on the process. To ensure that the etch recipe reached the buried oxide across SiCOI wafer, 3.6µm CD trench features on SiC wafers were etched to as deep as 57µm with etch rate of 635nm/min and taper angle of 88.5º, Figure 6. The main challenge of etching SiC at wafer level with nickel mask is a knifing effect (illustrated in Figure 7) that occurs due to variations in the thickness of electroplated nickel mask across the wafer. Ni mask recession near the feature edges can create a tapered mask that will exacerbate the issue. It was observed that the addition of an extra 500nm of nickel mask can avoid such damage to the trench opening. In Figure 8, the post-cleaning (using HNO_3) SEM image of HAR DRIE SiCOI sample presented the etch reaching buried oxide at 43µm depth with taper angle of 88.6º, footing < 100nm and sidewall roughness < 120nm. SiCOI wafer-level HAR DRIE resulted in successful fabrication of very high-Q > 2M gyroscopic disk resonators, limited by the thermoelastic damping due to roughness in the trench sidewall, with small as born frequency split, Figure 9. The frequency response of two degenerative modes of BAW disk resonator are shown in Figure 10.

DISCUSSION

The main challenge of transferring SiC DRIE from wafer pieces to the whole wafer is preserving the quality of trench profile while achieving good etch uniformity across the wafer. Lowering the pressure and increasing bias power enhance the etch uniformity; however, it comes at the cost of degrading mask selectivity and increasing sidewall roughness. In the following, several concerns with HAR DRIE of SiCOI are discussed.

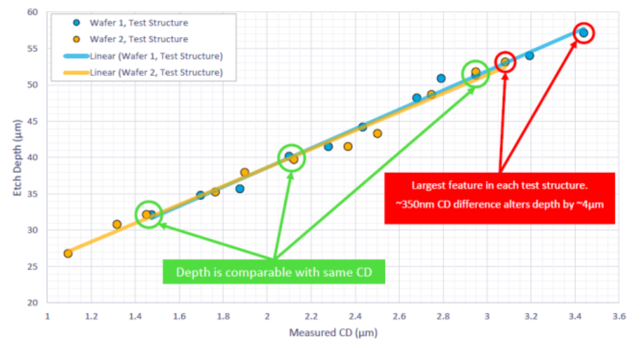

Figure 3: Plot of measured CDs on Ni mask vs etch depth (µm) after 65 minutes DRIE process on whole wafer SiC sample.

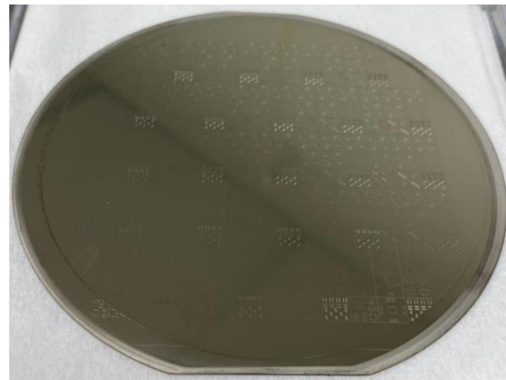

Figure 4: Optical image of a SiCOI substrate after high-aspect-ratio DRIE process using Omega® Synapse™ module.

Ni Mask Erosion and Critical Dimension (CD)

The reduction in mask selectivity can be mitigated by adding to the thickness of electroplated nickel. However, electroplated mask forms around the patterned photoresist, and its verticality depends on the cross-section profile of developed photoresist. Due to the nature of capacitive devices, our design desires a gap width of only a few microns, and 6µm thick electroplated nickel mask is needed to etch 40µm deep into SiC. Realizing such high aspect ratio photoresist with vertical sidewall is a crucial step in the mask preparation process, and therefore optimizing the lithography step prior to the electroplating nickel is a critical task.

It was also observed that achieving a high aspect ratio photoresist with complete vertical walls from bottom to top is a challenging task, since they usually tend to narrow down at the top of the photoresist feature. This feature non-ideality causes the CD to shrink in the case of over-electroplating. It worth noting that the mask thickness variation across the wafer also plays a role in CD variation changes at different location of the wafer based on the same principle.

Mask CD Variations and DRIE Lag Effect

The limits of deep reactive ion etching of high-aspect-ratio trenches into silicon carbide material using nickel mask was studied through various CD sizes, 1µm to 3.4µm, as shown in Figure 3. The lagging effect is pronounced for smaller CD sizes while trench aspect ratio slightly increases. The aspect ratio of 15:1 was achieved for 3.4µm openings while smaller CDs achieved higher aspect ratio of 20:1. The etch depth based on CD size assured that few hundreds of nanometer variations in CD size would not have significant effect on the etch uniformity.

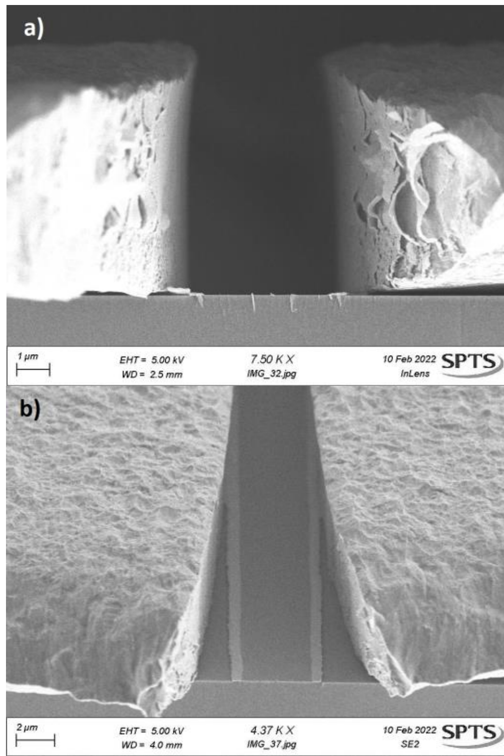

Figure 5: (a) Cross-sectional SEM image of electroplated nickel showing the mask sidewall is not completely vertical. b) Angled view of mask after cleaving which emphasizes the remaining seed layer caused by overhanging nickel during seed layer removal step.

Knifing Effect

As mentioned before, methods used to increase uniformity across a whole wafer reduces mask selectivity during etch processing. It is observed that mask is consumed at the trench opening faster than areas of blanket nickel. The knifing effect happened when trench opening loses the mask protection due to excessive recession of the nickel at the trench opening. The several stages of knifing effect are shown in Figure 7; it was seen this effect caused the passivation to peel off, damaging the trench opening and blocking plasma from the bottom of the trench. Since mask selectivity is calculated based on the mask bulk etch rate, it is not valid for the immediate vicinity of the trench opening. Therefore, it added further complication in defining mask thickness to successfully etch certain depth into SiC without damage to the trench opening while maintain good etch uniformity.

Notching/Footing Effect

In contrast to the knifing effect altering the trench opening at the top, the footing effect occurs at the bottom of the trench where silicon carbide meets underneath insulator layer. A low footing value of < 100nm was achieved on SiCOI wafers. It can be noted that etching SiC uniformly across the wafer is not the only key parameter to keep the footing minimized across the whole SiCOI wafer. The SiCOI device layer total thickness variation (TTV) also plays a crucial role in achieving minimum footing. A low TTV coupled with good uniformity from the etch process results in reduced overetch on the insulator layer, minimizing footing.

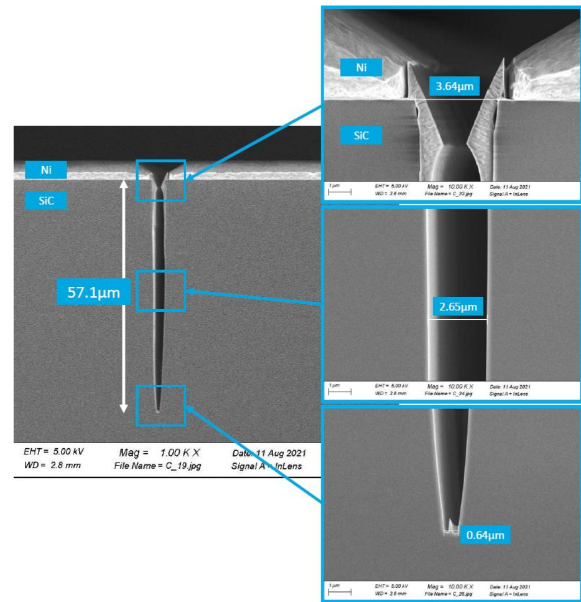

Figure 6: SEM image of HAR DRIE on SiC, it achieved aspect-ratio greater than 15:1 (57:3.6) with Ni mask selectivity of 28:1, 635nm/min etch rate and 88.5° taper angle.

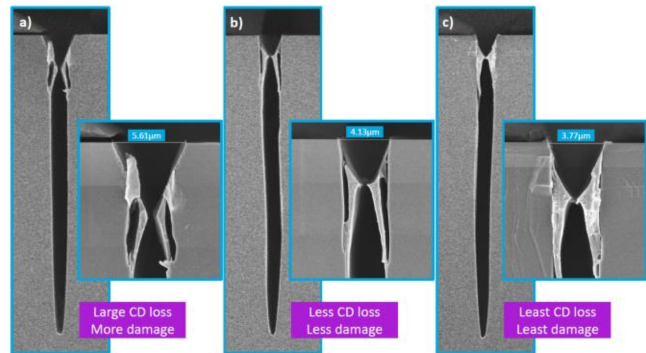

Figure 7: SEM of three different damage profiles caused by the mask thickness variation across the wafer, leading to knifing effect/passivation peel-off.

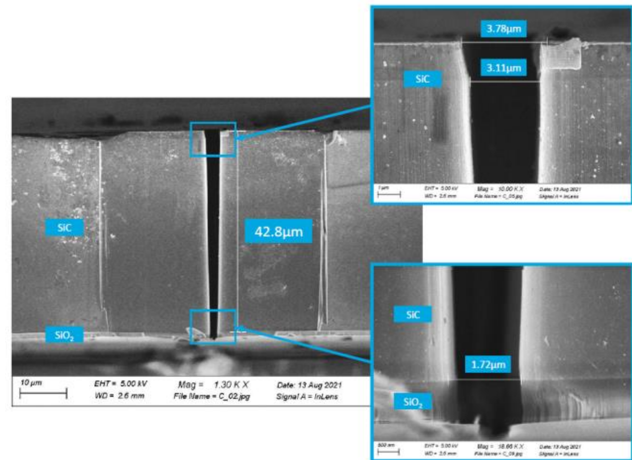

Figure 8: SEM image of HAR DRIE on SiCOI sample after cleaning process. Etch depth was 42.8µm with taper angle of 88.6°, footing < 100nm and sidewall roughness < 120nm.

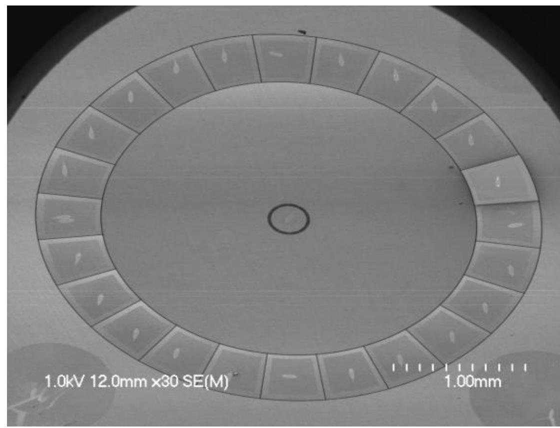

Figure 9: SEM image of a fabricated BAW disk resonator with Q > 2M from the wafer-level HAR DRIE on SiCOI substrate.

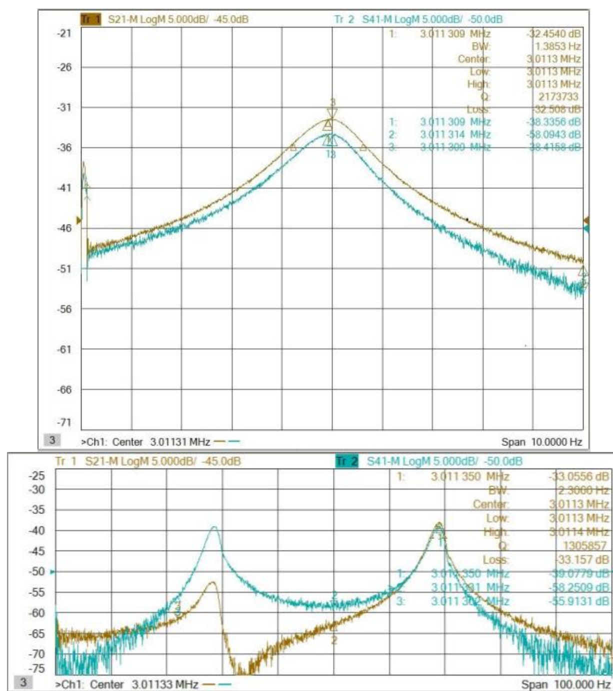

Figure 10: frequency response and Q measurement of the fabricated BAW disk resonator with Q > 2M from the wafer-level HAR DRIE on SiCOI substrate (top). Worst case frequency split of 40Hz measured for a 3MHz m=3 elliptical BAW resonator (~13.5ppm) on the wafer (bottom).

CONCLUSION

For the first time, the results of high-aspect-ratio (HAR) DRIE of thick 4H-SiC on Insulator (SiCOI) at wafer-level were presented. Using 6.5µm electroplated nickel mask, vertical trenches with aspect-ratios of 15:1 ~ 20:1 for CD size of only a few microns were achieved. The trench taper angle was 88.5º with a sidewall roughness less than 120nm, resulting in 4H-SiC bulk acoustic wave resonators with resonance quality factor greater than 2M at 3MHz. Even though the HAR DRIE of SiC faces several challenges consisting excessive mask erosion, mask CD variation and the knifing effect, the presented wafer-level results are a promising step to enable volume-manufacturing of ultra-high-Q monocrystalline SiC resonators.

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