LOW POWER 38.4 MHZ MEMS BASED REFRENCE CLOCK FOR QUARTZ REPLACEMENT WITH LESS THAN 30 PPM FREQUENCY STABILITY

Sarah Shahraini[1], Timo Huusari[1], Somnath Kundu[1], Hao Luo[1], Parvin Akhkandi[2], Yasaman Majd[2], Eduardo Alban[1], Brent Carlton[1], Ruth Vidana Morales[1], Jason Mix[1], Reza Abdolvand[2], Mohamed Abdelmoneom[1] and Nasser Kurd[3]

[1]Intel Labs, Hillsboro, OR, USA

[2]University of Central Florida, Orlando, FL, USA

[3]Design Engineering Group, Intel, Hillsboro, OR, USA

ABSTRACT

A 2.4 mW, 1ps RMS jitter temperature stable 38.4 MHz Thin Film Piezoelectric on Silicon (TPoS) MEMS based reference clocking chiplet implemented in Intel FinFET 22nm is presented as a viable traditional quartz crystal replacement. The TPoS full clock receiver comprises the TPoS resonator chiplet, pierce oscillator driver circuitry and the outer buffer converting the sinusoidal oscillation to a square digital clock. A 30ppm total frequency change across a temperature range from -40℃ to 120℃ is accomplished via a combination of passive compensation in the TPoS resonator structure and active temperature compensation using a fractional N Phase Locked Loop (PLL). Such competitive performance is achieved through a combination of the High-quality factor, low motional resistance, and the compensated composite structure of TPoS resonators along with design optimization of the 22FFL clock receiver circuitry.

KEYWORDS

Reference clock, MEMS contour mode resonator, Active temperature compensation.

TPOS RESONATOR DESIGN

Frequency scalable contour mode Scandium doped AlN on silicon TPoS resonator is designed as the frequency selective component of the oscillator demonstrated in this work due to their high-quality factor, low motional resistance, frequency scalability to few GHz and Quartz comparable ageing [1]. A third-order contour mode TPoS resonator is designed at 38.4 MHz as the reference clock to compare against performance of a 38.4 MHz industry standard off the shelf quartz crystal.

The resonators are fabricated on a relatively thick (20 µm) Ntype-doped <100> crystalline cut SOI topped with 1 µm sputtered 20% Scandium doped AlN film. The measured frequency response for this resonator is shown in Figure 1. Unloaded quality factor of 5.2k and motional resistance of 195 Ohms are measured at 38.38 MHz for this resonator.

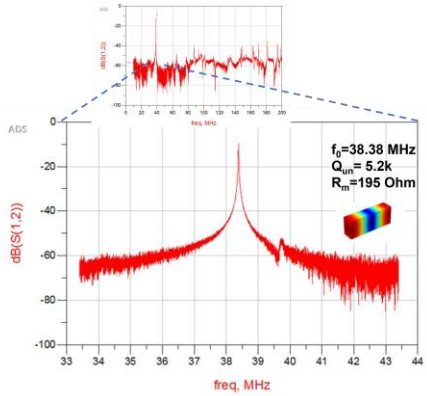

Figure 1: The measured frequency response for TPoS resonator (frequency selective component in the system).

A low level of passive temperature compensation is achieved with a lightly doped silicon layer yielding a temperature stability of about 1900 ppm for the extended temperature range (-40 ℃ to 120 ℃).

OSCILLATOR DESIGN

The oscillator architecture is shown in Figure 2. It consists of a Pierce oscillator core, an amplitude/bias control block, a voltage shaper, and a fractional-N PLL for active temperature compensation.

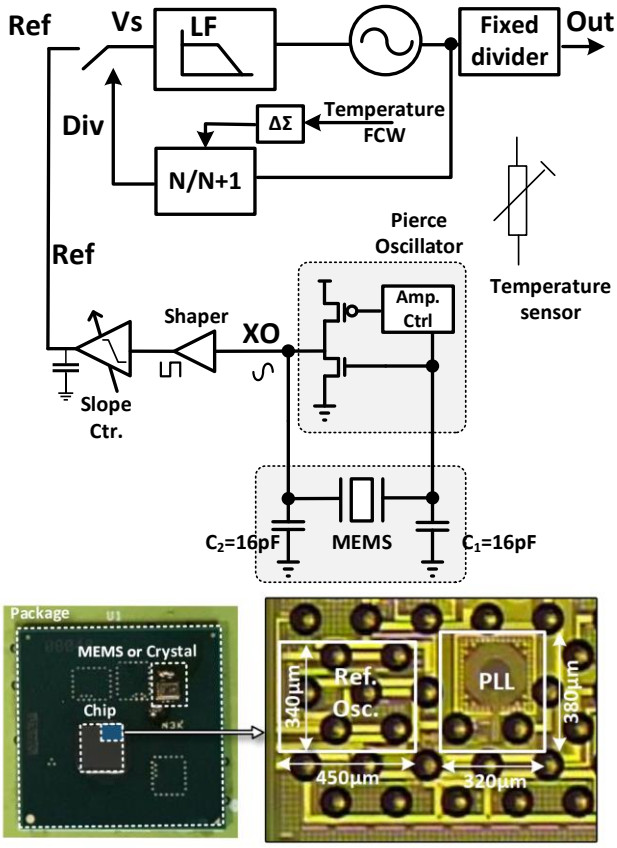

Figure 2: Architecture for the reference clock chiplet including, pierce oscillator core, shaper, fractional-N PLL, XTAL/MEMS and temperature senor.

The pierce core provides the negative resistance required to sustain the oscillation and the voltage shaper at the output of the Pierce oscillator converts the sinusoidal waveform to square wave to provide the clock reference for the PLL. A type-I sampling frac-N PLL is then used to compensate for the temperature dependent instabilities using a temperature sensor. The frac-N PLL has an output range from 2 to 2.48GHZ which is wide enough to cover

978-1-940470-04-7/HH2022/$25©2022TRF
DOI 10.31438/trf.hh2022.47

the MEMS temperature drifting range. The PLL's output clock is further Integer divided down to generate the target 38.4MHz output. MEMS resonator temperature drift error is corrected by changing the ΔΣ fractional word and hence the PLL's clock frequency. The PLL's 24 bit long fractional word is fine enough to correct the divided output clock within a 30ppm temperature stability.

MEASURED RESULTS

Measurement setup is shown in Figure 3. The same CMOS Pierce oscillator and driver are tested both with MEMS resonator and quartz crystal at 38.4 MHz for fair comparison.

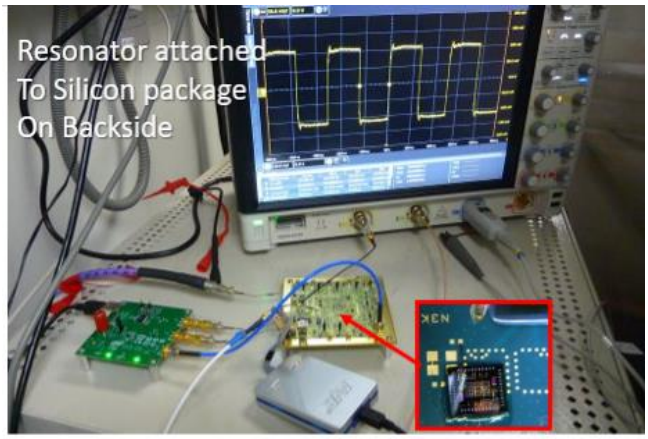

Figure 3:The measurement setup.

The measured RMS jitter (integration bandwidth 12kHz to 5 MHz) and clock signal power are plotted over temperature range of -40 ℃ to 120 ℃ and shown in Figure 4. The clock signal power reduces with increase in temperature while the integrated RMS jitter increases from a minimum of about 110 fs at -30 ℃ to a maximum of 220 fs at 120 ℃.

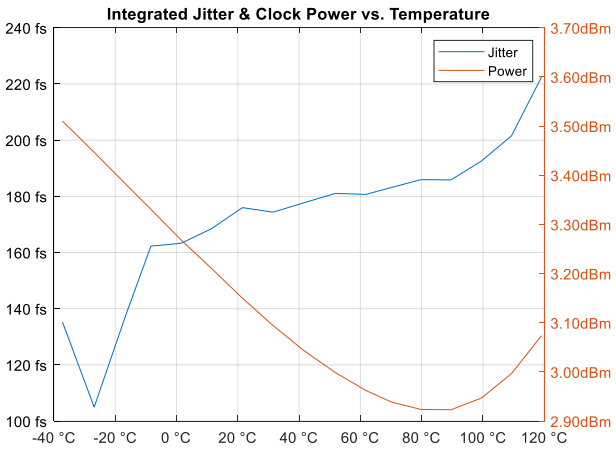

Figure 3: The measured RMS jitter (integration bandwidth 12kHz to 5 MHz with 4.1mW power) over a temperature range of -40 ℃ to 120 ℃. Clock signal power is also plotted over the same temperature range.

The frequency stability is also plotted in Figure 5 for the same extended temperature range with and without active temperature compensation. The frequency stability of the oscillator would be improved from 1900 ppm to less than 30 ppm by using active temperature compensation. The additional power consumption for the fractional N-PLL section is about 1.4 mW.

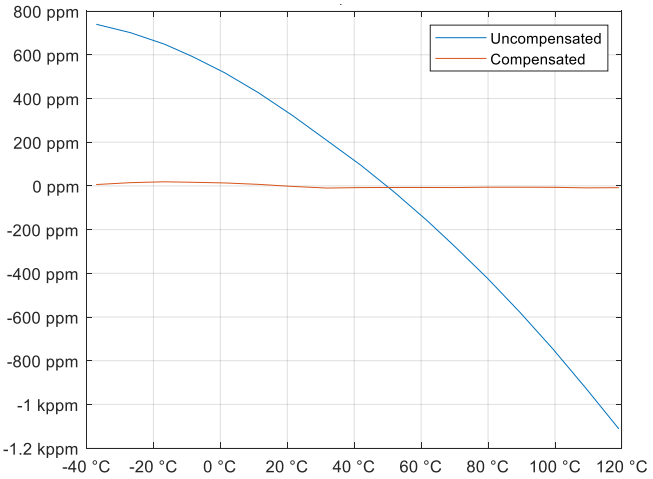

Figure 4: Frequency stability with and without active temperature compensation.

The performance for 38.4 MHz MEMS based and Quartz based reference clocks are compared at room temperature in TABLE 1. The presented demonstration clearly shows the viability of TPoS MEMS reference oscillators with similar performance as standard crystal oscillators with the key advantage of frequency scalability of the center frequency up to couple of GHz. This scalability could enable high frequency MEMS based reference clocks directly for high-speed IO systems and potentially eliminate the need for additional PLLs to save power and silicon area.

Table 1: TPOS MEMS based clock performance comparison to Xtal based Reference Clock

	38.4 MHz TPoS MEMS based Clock	38.4 MHz Xtal based Clock
Power	4.1 mW/1mW	3.9mw/1mw
Jitter (12KHz-25 MHz)	356 fs/1090fs	306 fs/841 fs
Startup Time	~ 75 µs	~ 292 µs/~ 60 µs (LCVCO start up [2])
Temperature stability (-40 ℃ - 120℃)	30 ppm (active compensation, additional 1.4 mW for ATC)	70 ppm

REFERENCES

[1] S. Shahraini et al., "Resilient Ultra Stable CMOS-MEMS Oscillator with Receiver in Intel 22FFL Technology," 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS), 2021, pp. 949-952, doi: 10.1109/MEMS51782.2021.9375330.

[2] H. Luo et al., "A Fast Startup Crystal Oscillator Using

Impedance Guided Chirp Injection in 22 nm FinFET CMOS," in IEEE Journal of Solid-State Circuits, vol. 57, no. 3, pp. 688-697, March 2022, doi: 10.1109/JSSC.2021.3136237.

[3] H. Luo et al., "A 12MHz/38.4MHz Fast Start-Up Crystal Oscillator using Impedance Guided Chirp Injection in 22nm FinFET CMOS," 2021 IEEE Custom Integrated Circuits Conference (CICC), 2021, pp. 1-2, doi: 10.1109/CICC51472.2021.9431500.

[4] S. Kundu et al., "A 2-to-2.48GHz Voltage-Interpolator-Based Fractional-N Type-I Sampling PLL in 22nm FinFET Assisting Fast Crystal Startup," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 144-146, doi: 10.1109/ISSCC42614.2022.9731560.

CONTACT

*S.Shahraini , sarah.shahraini@intel.com