A MEMS MICROVALVE FOR THE SPACECRAFT ATMOSPHERE MONITOR (SAM) INSTRUMENT

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ABSTRACT

This paper reports on the design, simulation, and characterization of a MEMS gas microvalve (MV) intended to be used as part of the Spacecraft Atmosphere Monitor (SAM) instrument, a highly miniaturized gas chromatograph mass spectrometer (GC-MS) for the International Space Station (ISS). All performance requirements at the system level were considered for flow and pull-in voltage simulations, and multiple tradeoffs were considered to ensure successful operation of SAM. Results of a selection of three MV generations are presented and discussed, including our latest generation, Rev ψ, that meets all the key performance requirements with significant margin with a measured sampling flow above 0.34 sccm and pull-in voltage below 255 V for a current lower than 1 μA.

KEYWORDS

Atmosphere monitor, International Space Station, ISS, gas chromatograph, gas valve, GC-MS, mass spectrometer, MEMS, microvalve

INTRODUCTION

The Spacecraft Atmosphere Monitor (SAM) instrument is a highly miniaturized gas chromatograph mass spectrometer (GC-MS), which can separate, identify, and quantify mixtures of chemicals completely autonomously. Over the years, SAM has undergone technological advancements for its potential application as an air quality monitoring instrument aboard the International Space Station (ISS). The first generation of SAM was deployed on ISS in July 2019 and had been monitoring the major components found in air: oxygen, carbon dioxide, nitrogen and methane, as well as checking humidity levels in real time [1]. The next generation of SAM, expected to launch by 2024, will also measure trace gases, using multiple MEMS components: a Pre-concentrator (PC), a Microvalve (MV), and a miniature Gas Chromatograph (GC) [2]. The MEMS PC and GC have already been tested as a sub-system, and results were presented in [3].

In this paper, we concentrated on the most challenging MEMS component of SAM, the MV, and the key SAM system requirements associated with it, which are:

1. electrostatically actuated with voltage and current limits of 300 V and 0.5 mA during operation,
2. being robust against 28 psi of pressure differential for all 5 moveable membranes,
3. minimum of 0.3 sccm of air flow across the system when PC is being loaded,
4. leak rate lower than 5e-5 Torr.l/s.

To meet these requirements, the MV has been through multiple design, fabrication, and test cycles, feeding achievable process and structural parameters back to optimize the overall MV design.

MICROVALVE DESIGN AND TOPOLOGY

The MV comprises of 4 layers (T-CAP, VC, MEM, and B-CAP) bonded using Au-Au compression bonding. T-CAP and B-CAP are 500 μm thick CZ silicon wafers, T-CAP is housing multiple microfluidic channels and gas inlets for Sample (S), Vent (V), Carrier (C), and the 2 gas ports to connect to PC. B-CAP is sealing the back of the 5 membranes and housing the Injection (I) port. The 5 membranes are independent electrostatic parallel plate actuators created across the VC to MEM interface. Both VC and MEM wafers are SOI (Silicon-On-Insulator) wafers, with a highly doped device layer and a FZ handle layer. Figure 1 shows a schematic of the MV chip, with an exploded view highlighting the geometry of the microfluidic channels, placement of the ports and location of the 5 membranes. Figure 2 shows the picture of a fabricated wafer along with an image of a MV chip and a scanning electron microscope (SEM) of a membrane on the MEM layer.

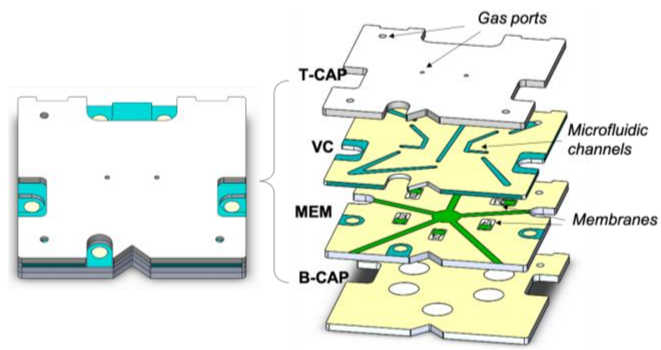

Figure 1. The MV chip and its exploded view, showing the 4-layers (T-CAP, VC, MEM and B-CAP) as well as the gas ports, microfluidic channels and the 5 membranes.

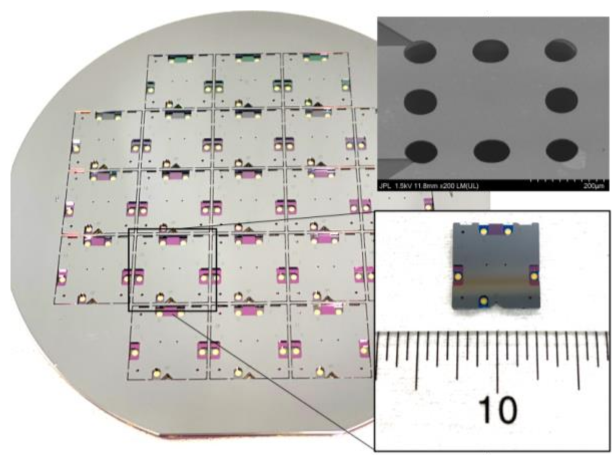

Figure 2. Fully fabricated wafer with multiple MVs. Insets show an SEM image of a membrane on the MEM layer and an individual MV.

Membrane design considerations were reported in detail in [4], including strategy to meet SAM requirements #1 and #2. Two membrane designs were simulated and fabricated, a 300 μm wide MEM design (300MEM) and a 400 μm wide MEM design (400MEM); images of both membrane designs are presented in Figure 3. The other requirements are explained in more detail in the following sections.

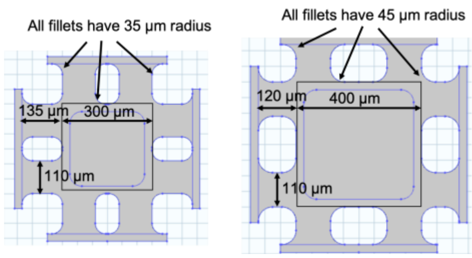

Figure 3. Design geometry for the 300MEM (left) and the 400MEM (right). Both were fabricated and tested against the SAM requirements for the MV.

SAMPLING FLOW REQUIREMENT

During sampling, the cabin air is being pulled from the sampling port, across the S-MEM, through PC, across the V-MEM, and through the vent port with a sampling pump (from TCS). Figure 4 shows the schematic of the system for that step, with the flow path highlighted in green.

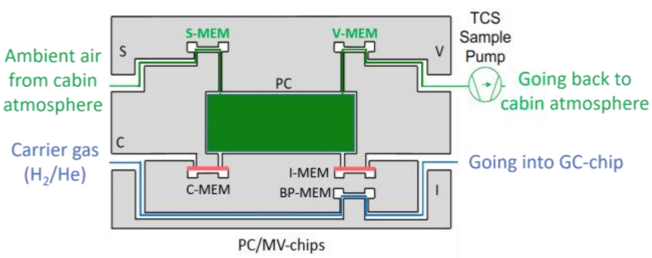

Figure 4. Simplified representation of the sampling step during SAM operation. The PC is being loaded with the ambient air using a TCS sample pump (green path). S-MEM and V-MEM are in the open position, while C-MEM and I-MEM are closed. Carrier gas is being pushed into the GC-chip via the BP-MEM (blue path).

The laminar airflow in the MV channels was modeled using COMSOL Multiphysics software (version 5.6). Simulations were performed for different pressure drop scenarios across the whole system. CAD designs were imported, domains for flow were defined, and flow equations with fine meshing were used to obtain the various flow rates. Figure 5 shows a 3-D representation of the PC-MV system, with microfluidic channels and the pressure difference plotted for the S-MEM and the V-MEM.

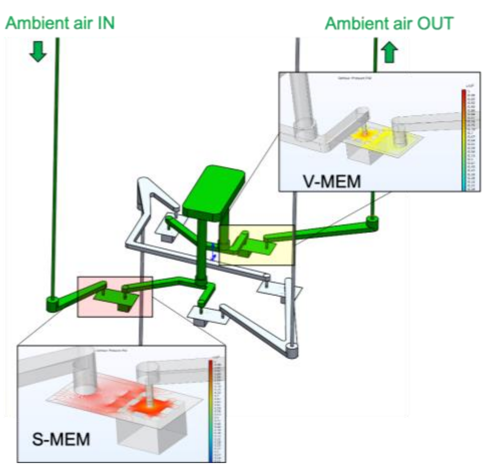

Figure 5. 3-D representation of the PC-MV microfluidic channels during sampling step (green path). Pressure difference across the system is simulated with close-up views on S-MEM and V-MEM.

The gap between VC to MEM and the diameter of the gas ports play a significant role on the sampling flow. Gas ports diameters ranging from 50 µm to 300 µm were considered, to accommodate higher flow while keeping the fabrication protocol feasible.

Another important parameter is the overall pressure difference created by the sampling pump, and how the pressure is distributed across the system. Early testing showed that the two membranes on the sampling flow path (S-MEM and V-MEM) could become deformed, and thus their design/sizing would impact the overall sampling flow if they were too flexible. Testing of MV Rev α showed that the sampling pump, while running at 5V, was creating a roughly 5 psi pressure difference across the whole system. This value was used to calculate the pressure difference for each membrane, for each VC-MEM gap, and ports sizing combination.

Additional COMSOL simulations were performed for both MEM designs, and pressure differences for a valve ranging from 1 psi to 3 psi, to simulate the membrane deformation for each case. We used a pressure profile across the valve similar to a truncated pyramid, divided each design in 50 µm squares (10×10 matrix for 300MEM, 14×14 matrix for 400MEM), and run the simulations assuming 100 µm diameter gas ports.

Figure 6 shows how the membranes were segmented, with each segmented boundary seeing some percentage of the total pressure load, and the resulting membrane deformation for 1 psi and 3 psi pressure difference for a valve.

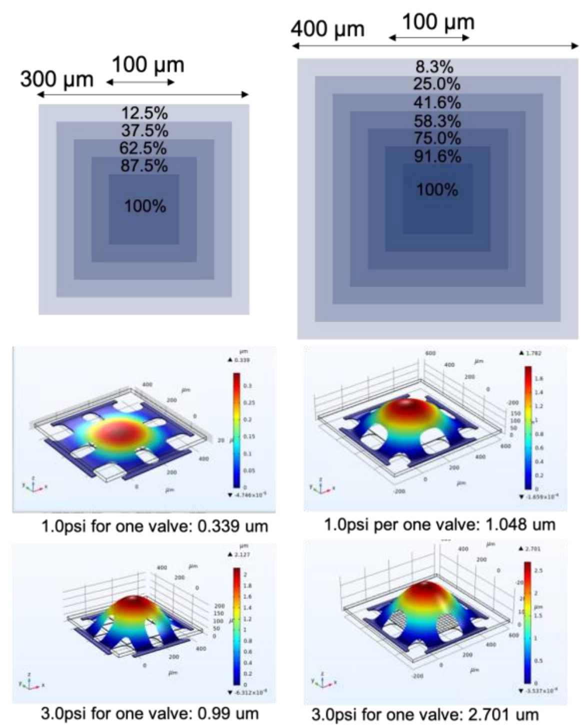

Figure 6. Membrane deformation for each valve were simulated using a segmented matrix and a gradual phasing of the pressure difference across the valve. Values for 1 psi and 3 psi are plotted for both 300MEM and 400MEM.

Figure 7 and Table 1 show a summary of simulated sampling flow for various gaps, various membrane geometries, and port sizing, with the expected membrane deformation for each case based on the pressure difference for each valve.

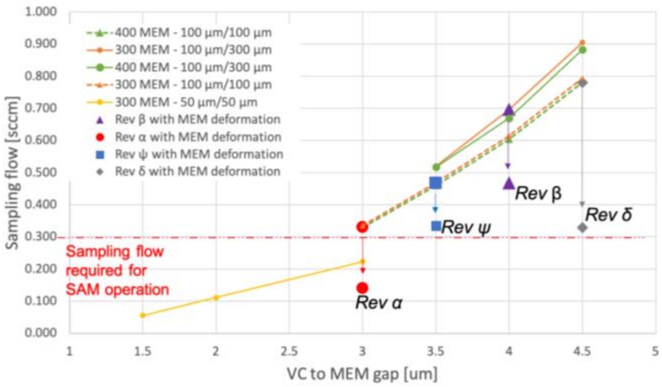

Figure 7. Simulated sampling flow at 5 psi pressure difference across the system, for various MEM sizing, holes sizing and VC to MEM gaps. The expected sampling flows, taking into account the deformation of the movable membrane, are also plotted for a selection of 4 MV generations.

Table 1. Simulated pressure difference across S- and V-MEM and resulting MEM deformation for various designs, assuming 5 psi pressure difference across the system.

Rev ID	MEM design	Hole sizing	VC to MEM gap	Pressure difference across S-MEM and V-MEM (each)	Expected MEM deformation
Rev α	400MEM	100 µm / 100 µm	3 µm	2.1 psi	~ 2 µm
Rev β	300MEM	100 µm / 300 µm	4 µm	1.6 psi	~ 0.56 µm
Rev ψ	300MEM	100 µm / 100 µm	3.5 µm	1.7 psi	~ 0. 57 µm
Rev δ	400MEM	100 µm / 100 µm	4.5 µm	1.8 psi	~ 1.7 µm

VOLTAGE AND CURRENT REQUIREMENTS

Electrical system requirements for the MV chip are listed as voltage and current limits of 300 V and 0.5 mA during operation. The proposed MVs are parallel-plate electrostatic actuators that would close when a voltage above the pull-in level but below the maximum allowable supply voltage (300 V) is applied.

A single MV can then be modelled as a parallel-plate actuator and pull-in voltage (V_{pi}) can be estimated using the following equation,

$$V_{pi} = \sqrt{\frac{8k_{eff}d^3}{27\varepsilon A_{eff}}}, \qquad (1)$$

where k_{eff}, d, ε, and A_{eff} are the effective stiffness, equivalent air gap, permittivity of air, and effective electrode area. Expected pull-in voltage for different revisions of MVs are shown in Table 2.

Table 2. Comparison of measured sampling flows and pull-in voltages with simulations, for a selection of 3 MV generations.

Rev ID	Simulated flow for VC to MEM gap	Simulated flow taking into account MEM deformation	Measured sampling flow	Simulated pull-in voltage with no pressure difference	Measured pull-in voltages
	ΔP = 5 psi	ΔP = 5 psi	ΔP = 5 psi		
Rev α	0.329	~ 0.140	0.035 – 0.178 (20 microvalves measured)	100 V	70V – 130 V (20 microvalves measured)
Rev β	0.699	~ 0.468	0.429 – 0.462 (10 microvalves measured)	280 V	240 V – 350 V (10 microvalves measured)
Rev ψ	0.468	~ 0.335	0.331 – 0.371 (10 microvalves measured)	224 V	220 V – 255 V (10 microvalves measured)

While electrostatic actuators do not draw much current in ideal conditions, unintended low resistance paths between the membranes or within the layers of MV chip can lead to leakage currents exceeding 0.5 mA. Therefore, electrical mapping of all connections VC-MEM and MEM-MEM is performed through I(V) traces, showing currents lower than 1 µA and all resistances above 500 MΩ.

LEAK-RATE REQUIREMENT

To ensure proper operation of the full SAM system, the overall leak-rate of the MEMS PC+MV+GC chain needs to be lower than 5e-5 Torr.l/s. The leak rate of the MV is measured by pumping the MV through the I port (while S/V/C and PC ports are physically plugged,), with a leak detector for 30 min and then inserting the whole block into a Helium filled bag. Helium will penetrate through the block and the MV and once the rate is stable for more than 30min, the leak test is completed.

With our none-ideal wafer bonder tool, we see a large difference in measured leak rates, between the dies at the periphery of the wafer and the dies at the center of the wafer. Thermal analysis of the temperature gradient across the full stack during bonding informed us that there is a loss of about 15 ^{0}C from the side of the wafer to the center of the wafer, which would impact the Au-Au compression bond quality and in turn negatively impact the leak-rate. One way to improve the leak rate is to epoxy seal the periphery of the MV, which has shown to reduce the leak rate by a factor of 10 to 50 times.

REVα AND REV β DISCUSSION

As explained in the leak-rate section, the wafer-level bonding quality is a key factor to have operational MVs, with sampling flow and pull-in voltages being highly dependent on the VC to MEM distance. If the bonding is poor, the VC and MEM plates can be further apart, which will give more flow but will also drive the pull-in voltage higher. This was our main issue for MV generation Rev α and Rev β, and why most of the MVs in Rev β were not meeting the pull-in voltage requirement.

The other very important aspect is the removal of the buried-oxide (BOX) under the membrane, on the MEM SOI wafer. If the BOX is not completely removed, and some oxide is left on the corners/legs of the movable membranes, they will buckle up. This will play against the VC to MEM distance, thus lowering the sampling flow and the pull-in voltage. This was the second issue affecting MV generation Rev α, and it explains why both sampling flow and pull-in voltages for that generation were so wide spread. Experimental results for those two generations are summarized in Table 2.

REV ψ FABRICATION PROCESS AND RESULTS

Learning from our experience and from all our various simulations, we fabricated the final round of MV Rev ψ. For this fabrication run, the 300MEM was selected, with a 3.5 µm physical gap before membrane deformation. When taking into account the ~0.56 µm membrane deformation, the physical gap during sampling would be a little less than 3 µm, for an expected sampling flow of 0.335 sccm.

All 4 layers of the MV are fabricated on 4-inch (100 mm) wafers, using conventional photolithography processes, combined with Fluorine-based ICP for any oxide etching and Deep Reactive Ion Etching (DRIE) for any silicon etching:

- Both T-CAP and B-CAP wafers have an initial step of Cr/Pt/Au lift-off process followed by silicon DRIE on the top side and bottom side of the wafers.

- On the VC SOI wafer, silicon DRIE is performed first on both sides, to define the pillars, the electrical plate and the through holes, followed by the growth of 1 μm of thermal oxide to ensure electrical isolation of all the structures. Subsequent steps include removal of the BOX and TOX (Thermal Oxide) layers with Fluorine ICP and Cr/Pt/Au lift-off process on both sides of the wafer, followed by a final silicon DRIE step on the top side.
- On the MEM SOI wafer, each membrane island is defined first, followed by growth of 2 μm of thermal oxide for electrical isolation. Subsequent steps include removal of the TOX layer with Fluorine-ICP and Cr/Pt/Au lift-off process on both sides of the wafer, followed by silicon DRIE on the top side to define the membranes, and silicon DRIE/Fluorine ICP on the bottom side to remove the silicon and BOX underneath the membranes.

Flatness of the membranes are confirmed using a Veeco Wyko optical profilometer and I(V) traces are performed to confirm MEM-MEM electrical isolation before bonding. All four wafers were bonded at once; we performed a wafer-to-wafer manual alignment under an infrared (IR) microscope, and we bonded at 320 ^{0}C, using 20 kN force for 16 hours.

For Rev ψ, the pull-in voltage was simulated at about 224 V. 15 MVs were measured and results are included in Table 2. Most of the MVs on the periphery of the wafer showed excellent leak-rates of 1e-6 Torr.l/s or lower, sampling flow of 0.34 sccm and pull-in voltages of 230 V. The MVs located towards the center of the wafer, that showed higher leak rates, were epoxy sealed to meet the leak rate requirement. More than 90% of those MVs exhibited a leak rate better than 2e-5 Torr.l/s post-epoxy. They also have a slightly higher sampling flow and pull-in voltages, as expected, but still meeting the SAM system requirements.

Figure 8 presents a typical flow measurement performed as part of our acceptance tests, with cycling of a V-MEM on one of the tested dies from Rev ψ, using 230 V as the pull-in voltage, and showing gas flow being stopped when the membrane is actuated.

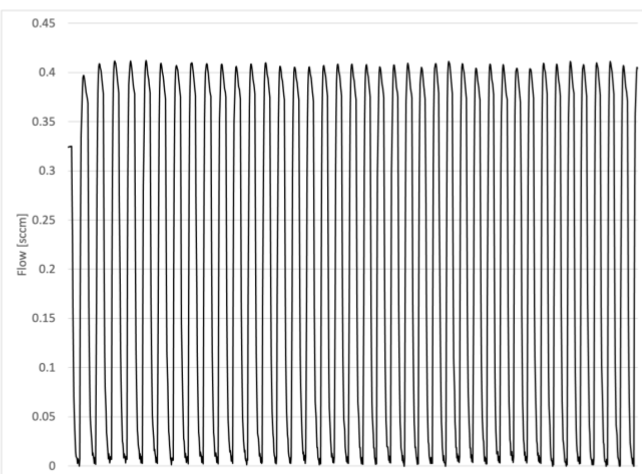

Figure 8. Cycling of a V-MEM from Rev ψ, at 230 V. The membrane is commanded "close" for 20 sec (230 V applied), then commanded "open" for 20 sec (0 V), and both commands are looped for 40 cycles.

CONCLUSION

In this paper, we reported on the development of a MEMS gas microvalve (MV) for the Spacecraft Atmosphere Monitor (SAM) instrument. Focusing on the key system parameters associated with the MV, we carefully simulated, designed, and fabricated a MV that could provide a sampling flow above 0.3 sccm, with a voltage and current below 300 V and 0.5 mA respectively and a leak rate of less than 5e-5 torr.l/s. Our latest MV generation, Rev ψ, provides a sampling flow above 0.34 sccm, a pull-in voltage below 255 V, a current below 1 μA, and a leak rate better than 2e-5 Torr.l/s. This MV generation is now being assembled with the rest of the SAM MEMS components, the PC and the miniature GC, with the full SAM instrument expected to be launched to the ISS by 2024.

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