MANUFACTURING NEXT-GENERATION MICROELECTRONICS

Carl E. McCants
Defense Advanced Research Projects Agency (DARPA), Arlington, Virginia, USA

ABSTRACT

At the 2021 DARPA Electronics Resurgence Initiative (ERI) Summit and MTO (Microsystems Technology Office) Symposium, plans for the next iteration, named ERI 2.0, were discussed. One of the areas DARPA is planning to pursue is manufacturing complex 3D microsystems. The R&D needed for advanced microelectronics manufacturing would include the design, assembly, testing, and digital emulation of 3DHI (3-Dimensional Heterogeneous Integration) microsystems, with an emphasis on: a) Multi-chip, multi-technology assembly and packaging; b) Tools for design, simulation, and test; c) Security; d) 3DHI interconnects; and e) Thermal management and power delivery. This paper will discuss challenges related to manufacturing complex 3D microsystems.

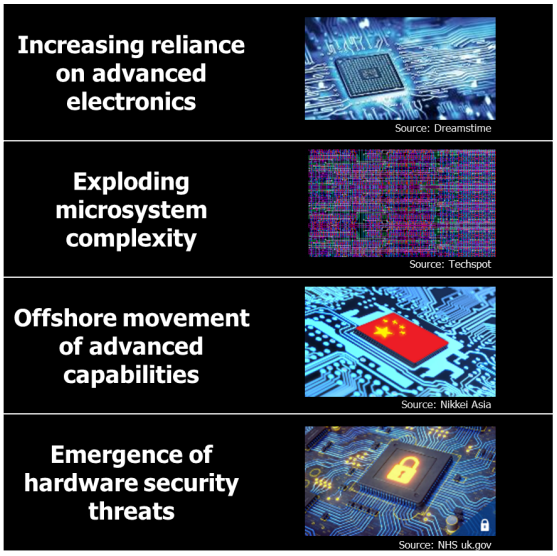
KEYWORDS

3DHI, advanced microelectronics, multi-chip packaging.

INTRODUCTION

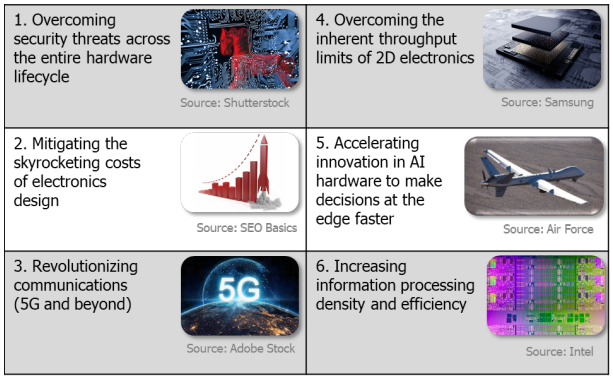
ERI History

ERI had its genesis 5 years ago with the recognition that continued US leadership in microelectronics was threatened in both the defense sector and commercial industry. In January 2017, the President's Council of Advisors on Science and Technology, or PCAST, issued a report titled "Ensuring Long-Term U.S. Leadership in Semiconductors". The report stated the following: 1) U.S. semiconductor innovation, competitiveness, and integrity face major challenges; 2) A concerted push by China to reshape the market in its favor, using industrial policies backed by over one hundred billion dollars in government-directed funds threatens the competitiveness of U.S. industry and the national and global benefits it brings; and 3) The United States will only succeed in mitigating the dangers posed by Chinese industrial policy if it innovates faster.[1] Out of this came four major factors (Figure 1):



1. The increased reliance on and strategic importance of advanced electronics for national security and economic competitiveness. Microelectronic components are found in everything from toasters to televisions, mobile platforms to automobiles, but also aircraft to satellites.
2. The exploding complexity of microsystems that we see in state-of-the-art CPUs, GPUs, FPGAs, and other System-on-chip/System-in-package configurations.
3. The offshore movement of advanced manufacturing capabilities.
4. The recognition and emergence of hardware security threats that can impact the confidentiality, integrity, and reliability of microelectronics used in both consumer and defense applications.

From these four factors, six focus areas were proposed as seen in Figure 2:



- Overcoming security threats across the entire hardware lifecycle
- Mitigating the skyrocketing costs of electronic design
- Revolutionizing communications (5G and beyond)
- Overcoming the inherent throughput limits of 2D electronics
- Accelerating innovation in AI hardware to make decisions at the edge faster
- Increasing information processing density and efficiency

ERI Present

In looking back at where we were in 2017 and where we are today, those factors appear even stronger than they did when ERI was initiated, with new trends emerging, and consensus need for action to address some of these trends, which include:

- Enormous off-shore investments in commercial electronics by near-peer allies and adversaries have only grown since the start of ERI, particularly as manifested by the consolidation of leading-edge silicon manufacturing and an increasing footprint into state-of-the-art packaging by pure-play foundries[2]

- Microelectronics supply chain integrity concerns, spurred by the disruptions due to COVID-19 and the global nature of the supply network[3]
- The formation of multinational alliances for 3DHI R&D and manufacturing[4]

The result is that ERI will continue to strategically invest and seed new approaches and technologies to maintain the U.S. position in electronic systems. In addition, recognition of the importance of microelectronics technologies has been increasing dramatically within the DoD and other government agencies. Finally, substantial investment in microelectronics has been identified as a key priority within not only the DoD, but across the whole of government. [5]

ERI Highlights

Since its inception, ERI has increased participation of non-traditional partners from commercial industry in DARPA programs. ERI has fostered collaborative projects involving 6 of the top 10 semiconductor sales leaders. In addition, ERI has fostered collaborative projects involving all 5 top defense contractors and all of the top 10 research universities per US News & World Report rankings. More importantly, dialogue has increased with many of these entities, although we are still striving to increase the base of those participating in our funded research (Figure 3).

Research successes in ERI over the past year include processor architectures that are >100X faster than standard CPU/GPUs (HIVE); development of programmable hardware architectures to increase processing efficiency (SDH); integration of machine learning into tools for end-to-end electronics design (IDEA); data privacy research to process information while it remains encrypted such that data is protected (DPRIVE); FETT Bug Bounty, DARPA's first crowdsourced leveraging of "white hat" hackers (SSITH); Integration of an FPGA core with a photonic transceiver in a multi-chip module (PIPES); early demonstrations of 22nm FinFETs for specific Defense Industrial Base (DIB) applications (Domestic Foundries); and provided open licensing with commercial technology vendors to DARPA researchers (DARPA Toolbox). In addition, over the past year, we have created several new ERI programs in computing, algorithms, filters, and heterogeneous integration.

MANUFACTURING COMPLEX MICROSYSTEMS

ERI Future Plans

With the benefit of hindsight, ERI has demonstrated that it is possible to engage the academic, commercial, and US Government microelectronics communities in relevant, cutting-edge, dual-use research projects. It is also possible to provide leap-ahead capabilities in computational efficiency, heterogeneous integration, hardware security, electronics design, AI components, and secure communications through these collaborations that benefit both the USG and private sector. However, maintaining technical advantage will require continuous innovation, and maintaining US supremacy in semiconductor technologies over the long-term will demand national investment in disruptive technologies. A fundamental assumption that informed the direction of ERI 2.0 is that future microelectronics innovation will not be driven by transistor scaling but will instead be tied to the ability to design, fabricate, and test and model the performance of complex 3D assemblies composed of heterogeneous microelectronic technologies. [6-9] In that context, lab-to-fab capability also represents an opportunity and the potential to accelerate and re-shore future manufacturing.

Taking all this into account, in ERI 2.0, DARPA MTO will continue innovating the next generation of microelectronics through the initial six areas and add two new areas. The first area is R&D for advanced manufacturing. This includes the design, assembly, testing, and digital emulation of 3DHI microsystems, with an emphasis on the following:

- Multi-chip, multi-technology assembly and packaging
- Tools for design, simulation, and test
- Security
- 3DHI interconnects
- Thermal management and power delivery

The first area also includes developing electronics for harsh environments – radiation, high temperature, high voltage or current, and low temperature.

The second area is next-generation microelectronics prototyping. The primary objective is to create a national capability for 3DHI by establishing a public-private partnership, or PPP, for research services and low-volume production. An additional objective is to emphasize design innovations and enhance the use of manufacturing automation in the package, assembly, and testing process. The expectation is that this will:

- Reduce cycle-time for R&D and pilot manufacturing for 3D electronics assembly
- Ensure a more secure supply chain with a domestic facility and capabilities driven by future industry needs
- Provide technology for advanced packaging and assembly, with the potential for significant cost reduction in microsystems

Advanced 3DHI R&D Challenges

Knowing the right question to ask, creating a viable path to transition, and focusing on manufacture – these lessons form a virtuous loop, in which manufacturing challenges help inform the next set of questions to go answer. Knowing the right question to ask is central to DARPA's ability to do its job well. Some examples we are thinking about at DARPA MTO now include:

- Will advanced interfaces (die-to-die, wafer-to-wafer, die-to-wafer, and so forth) obviate conventional fabrication and packaging?
- Would assembly approaches allow complex systems to be disaggregated into more basic primitives?
- How will dense 3DHI assemblies be designed and tested?
- Will new manufacturing technologies, like fine-scale printing and additive manufacturing, enable precisely aligned lateral interconnects and through-substrate-vias?

- How can the electronics within advanced 3D assemblies and packages be powered… and how can they be cooled?
- Are there new materials and thermal strategies to extend temperature operation range for 3D assemblies?
- How will multi-domain, integrated EDA tools for 3DHI be achieved?
- How can complete digital models of 3DHI systems be developed and validated?

This initial set of questions has led to the development of the following focus areas for 3DHI manufacturing:

- Multi-chip, multi-technology assembly / packaging
  - Compatible die-to-die, wafer-to-wafer, die-to-wafer, and wafer-to-board processes
  - Desktop assembly
- 3DHI interconnects
  - Precisely aligned lateral interconnects through fine-scale printing and additive manufacture
  - Post-commercial-3DHI TSVs (through-substrate-via)
- Thermal and power
  - Embedded thermal management within assembly and package
  - Materials to extend temperature operation range
  - Low-loss passives for power distribution
  - Efficient power conversion in assembly / package
- Tools for design, simulation, and test
  - 3DHI metrology
  - Multi-domain, integrated EDA tools for 3DHI
  - Validation of complete digital models
- "MOSIS-like" 3DHI prototyping services
  - Baseline 3DHI fabrication processes
  - 3DHI multi-project and taxi run demos with ADK (assembly design kit)

Creating a viable transition path for these new technologies will be another central focus of ERI 2.0. In a world in which domestic production accounts for only 12% of chip manufacturing and just 3% of packaging, how do we create ways in which innovation can be developed and leveraged for commercial and defense applications? DARPA ERI 2.0 will address the question "How do we build a sustainable path for innovation to move from the laboratory to industry?"

As part of the manufacturing thrust, we will continue towards the goal of getting advanced technologies prototyped and into the hands of transition partners and users. This includes continuing to develop the microelectronics technologies in ERI and all of the MTO thrusts areas. We will also be working with our government partners, industry, and academia to determine if a public private partnership in advanced microelectronics manufacturing and heterogeneous integration is something we can make a reality over the next year.

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CONTACT

*Carl E. McCants, tel: +1-703-526-2808; carl.mccants@darpa.mil