TOWARDS A CMOS INTEGRATED PIEZOELECTRIC MEMS PROCESS DESIGN KIT

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ABSTRACT

Piezoelectric AlScN/AlN thin films have enabled the integration of CMOS and MEMS with a wide variety of MEMS devices. Compared with the CMOS fabless design/foundry manufacturing model, where a PDK with multiple different devices is available for designers, there are very few shared MPW piezo-MEMS processes, and there are none that can support multiple different types of devices. A Piezo-MEMS PDK would enable CMOS designers to make systems from piezo-MEMS devices, not just MEMS experts. A Piezo-MEMS PDK that utilizes libraries of MEMS transducers and circuits is needed to fuel the development of piezoelectric MEMS systems to broader CMOS and sensors/actuators communities. In this work, we demonstrate the development of a process flow that supports both released resonators and bulk coupled GHz bulk ultrasonic transducers. We demonstrate functioning devices that consist of GHz BAW, FBAR, and CMR devices.

KEYWORDS

AlN, AlScN, Piezoelectric, MEMS, PDK

INTRODUCTION

CMOS-based integrated circuits are based on the existence of Process Design Kits (PDK) which guarantees device performance for a multitude of devices. A typical CMOS process supports a variety of devices such as transistors, diodes, resistors, capacitors, and inductors and these devices are available as parametric cells (P-Cells) in a process development kit (PDK) that allow layouts and simulation models to be automatically generated for different device sizes – designers do not need to know how to perform TCAD or FEM modeling to use these devices. Furthermore, due to the limited number of thin film stack options that designers have access to, multi-project wafer (MPW) runs can be easily done, lowering the barrier to entry and allowing designers to prototype designs for a relatively low cost.

In the past, MEMS design kits have focused on electrostatic MEMS. These include the MUMPS and SANDIA SUMMIT processes. These processes had a significant impact on the MEMS community allowing vast penetration into research and commercial sectors. Similarly, CMOS integrated electrostatic MEMS has been a research focus and has yielded commercial successes [19, 21]. Generally, the packaging required for electrostatic MEMS, and the higher voltages prevents the technology from scaling to deep sub-micron transistors where supply voltages are limited to ~1V. Similarly, recently AlN/CMOS integration approaches have been implemented onto CMOS nodes up to 130nm. This technology node is still an older technology, which is not an active node for the CMOS community. This disparity prevents the accessibility of MEMS to the much larger circuit design community. Furthermore, MEMS processes, including MEMS on CMOS processes, are typically optimized for a single device type. Innovation is often on the device itself, and substantial FEM simulations of devices are conducted, as a typical design requires an extensive understanding of process parameters and device operation. There is no current equivalent MEMS on CMOS process/PDK that offers the same flexibility to support multiple types of devices, support for MPW runs, and the same ease of use for designers as a CMOS, at a CMOS node that is compatible with the vast majority of CMOS designs. Such a MEMS PDK, were it available, would enable any CMOS designer to make systems using MEMS devices – by making well-characterized P-Cells of MEMS devices available, incorporating MEMS devices into integrated circuits would be as simple as instantiating an on-chip inductor or MIM capacitor into a CMOS design today.

The target platform of choice for this work is aluminum nitride (AlN) based Piezo-MEMS process, as shown in Fig. 1. Integration of MEMS on CMOS offers several key advantages including reduced electrical parasitics allowing for higher SNR and lower power consumption, high interconnect density allowing for large sensor arrays, and reduced device form factor. While other MEMS technologies such as electrostatic MEMS are capable of being integrated into CMOS, Piezo-MEMS stands out in the sheer variety of devices enabled by thin film AlN/AlScN. The CMOS compatibility of AlN has enabled numerous MEMS devices to be integrated onto CMOS, including FBAR resonators [1], piezoelectric micromachined ultrasonic transducers (PMUT) [2], piezoelectric transformers [3], contour-mode resonators (CMR) [4], microphones [5], and GHz ultrasonic transducers [6-7]. Other devices enabled by thin film AlN or AlScN include piezoelectric gyroscopes [8], optical waveguides and modulators [9], RF switches [10], and ferroelectric memories [11], among many others.

For a MEMS thin film stack to be suitable for a common PDK platform with the possibility of MPW runs, the allowable layer thicknesses must be restricted to a limited number of variations, much as how CMOS processes allow designers only a limited choice over metal layer thicknesses. Therefore, the target devices supported by the PDK must primarily have their functionality determined through layout/lithography, and not through changing layer thicknesses.

As a result of these considerations, the target devices chosen for the PDK are CMRs, PMUTs, and GHz transducers. These devices all feature significant amount of functionality that is lithographically "programmable." For CMRs, their resonance frequency is determined by their electrode spacing [12]. PMUT center frequency is determined by the transducer radius [13]. The center frequency for GHz transducers is set by the AlN and top dielectric thin film layer thicknesses, but several key functions are lithographically definable such as adjusting acoustic beam width through transducer sizing, adjusting echo amplitudes through transducer spacing, and adjusting diffraction characteristics through layout [14]. This flexibility allows GHz transducers to be used in a variety of configurations such as for GHz ultrasonic imaging [15], ultrasonic communication channels [16], temperature sensing [17], and clock oscillators [18]. By allowing users some choices in AlN and top dielectric layer thicknesses, more control over device operating frequencies can be realized. In addition, due to their commercial relevance and because a release step is supported as part

978-1-940470-04-7/HH2022/$25©2022TRF
DOI 10.31438/trf.hh2022.7

of the process, released membrane resonators such as FBARs can be realized on the process.

THIN FILM LAYER STACK

The process was developed at the Cornell NanoScale Science and Technology Facility (CNF) and the thin film layer stack chosen for the process is shown below. The choice of layers starting from bottom to top are 1) SiO2 release layer (1000 nm), 2) AlN buffer layer for electrical insulation purposes (50 nm), 3) bottom Ti/Pt electrode (100/20 nm), 4) AlN piezoelectric layer (0.5, 1 and 1.5 µm), 5) top Ti/Al electrode (200/20 nm), and 6) top Si_xN_y buffer layer (300-900 nm). The process was fabricated on both 4-inch wafers and 8-inch wafers. 4-inch wafers are more convenient for fabrication in CNF due to more tool compatibility. The same process

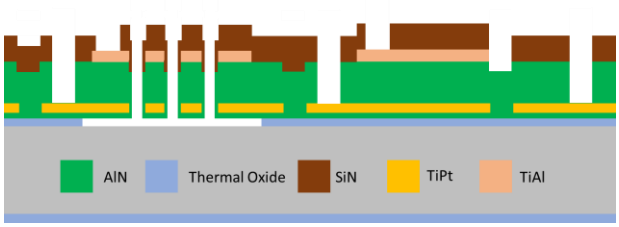


Figure 1. Cross-section of the Piezo-MEMS process flow

was also run with 8-inch wafers, due to the need to develop a process that can work with 8-inch CMOS wafers. This choice of layer stack up allows for both released devices and bulk coupled GHz transducers. GHz transducers and resonators can also be realized by a top dielectric etch above the devices to remove the nitride above the top electrode of the devices.

MASK LAYOUT

The reticle layout is shown in Fig. 2, where a 10 x 10 mm reticle size has been chosen to allow for 1x4 multilayer masks to be used. Devices included on the reticle include several variations of GHz transducer devices, PMUTs, CMR resonators, FBARs, piezoelectric in plane bimorphs, and process calibration structures.

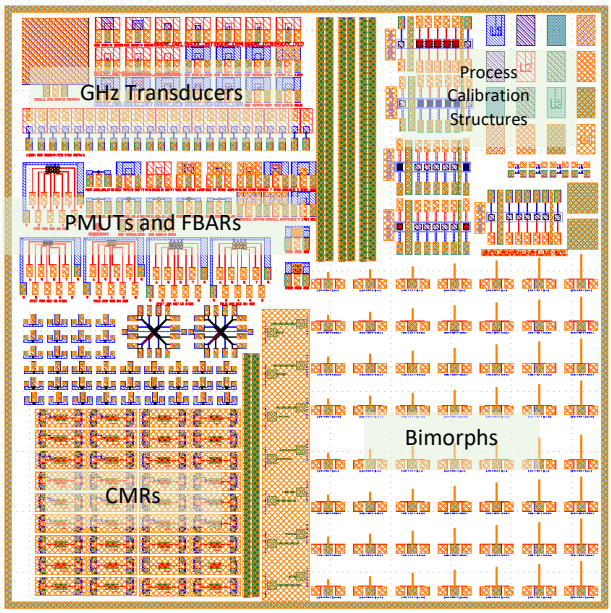


Figure 2: Mask Layout

DEVICE FABRICATION AND PROCESS FLOW

An ASML 248nm DUV process was used to achieve the required resolution (~400 nm) where the tool is compatible with both substrate sizes (100 and 200 mm). The UV210 DUV positive resist (500 nm) with UV42P antireflection coating (62 nm) is applied by an automatic Suss MicroTec Gamma cluster for all layers. Standard (ASML Combi reticle) PM and SPM_X, and SPM_Y ASML marks are used for alignment between layers. New alignment marks are added to each new layer and used for aligning process in the next layer.

The process starts with thermal oxides (1000 nm) grown on DSP Si substrates. As this process is intended as a feasibility study, release layer patterning and planarization steps were not performed, thus resulting in the need to do timed etch release (different for each set of devices) which results in nonuniformities in the release cavities. Next, a thin (50 nm) isolating bottom AlN layer was deposited with an OEM Endeavor M1 40kHz ac reactive sputtering system. A Pt/Ti (100/20 nm) film was deposited with the DC sputtering process for bottom electrode metallization. The Pt film deposition process was optimized to achieve XRD-RC of ~3-3.5 deg (FWDM). The bottom electrode was patterned with 1st mask and was patterned using the multi-step Ion Beam Etching (IBE) process (AJA International). A multiangle process was utilized to remove the fencing artifact in the IBE process. Then the AlN piezo layer was deposited while the film stress for each thickness was precisely tuned to be as close as neutral using the Stress Adjustment Unit (SAU, resistor box) in the Endeavor M1 system. The stress measurement was performed using two angles (FleXus) and carried out to keep the total wafer bow under 40 µm to avoid handling issues with robot transfer systems.

The top electrode metallization (Ti/Al) was deposited using DC magnetron sputtering and was patterned by 2nd mask layer. The top electrode patterns are etched by the ICP-RIE process (Plasma-Therm 770) using Cl2 and Ar chemistry with added CH4 for

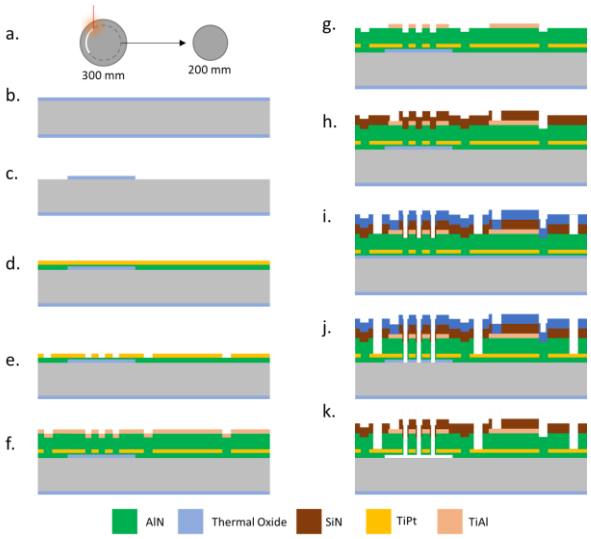


Figure 3. The process flow with released and solidly mounted AlN transducers and SixNy buffer layer for bimorphs. Thickness of ALN is 1.5µm, thickness of SixNy is 0.9µm.

sidewall profile control, followed by a short SF6 exchange reaction step to avoid corrosion of Al patterns (due to instability of AlCl3). Then the elastic layer (SiN) was deposited using the PECVD process and a tight film stress control to achieve minimized (<+/- 50 MPa) residual film stress. The SiN layer was patterned by the 3rd mask layer and was etched using the ICP process (Oxford 100) in Ch2F2

plasma chemistry to achieve vertical sidewalls. Then, a hard mask deposition and a Cl2-based ICP process were used for etching AlN film (4th mask) for access to the bottom electrode and access to oxide (release holes). The AlN etch process was developed to achieve highly vertical sidewalls and minimize sidewall erosion effects [20].

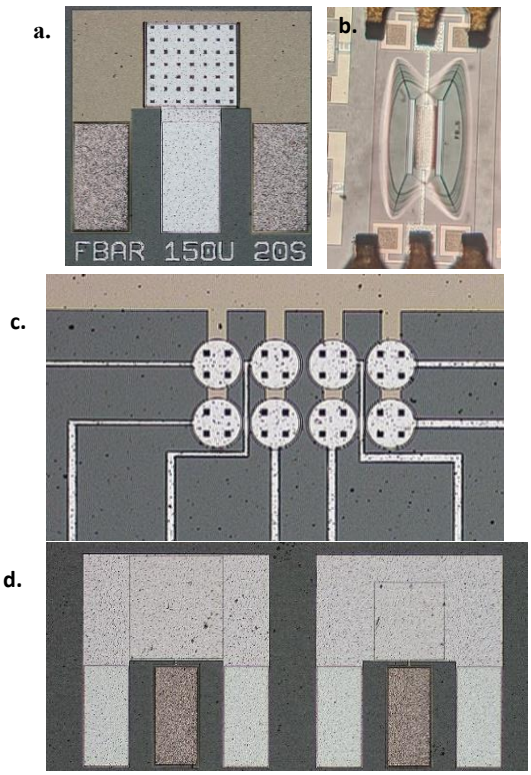
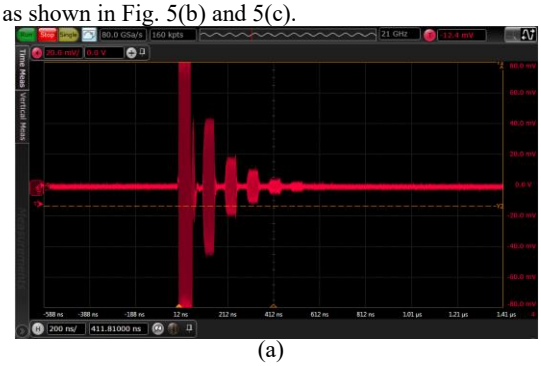


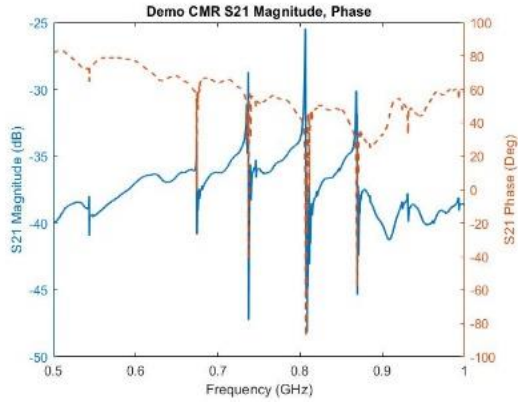
Figure 4. Fabricated devices (a) FBAR (150x150µm), (b) CMR (150x100µm), (c) PMUTS (2x4 array, R=50µm, (d) GHz transducers (200µmx200µm).

MEASUREMENT RESULTS

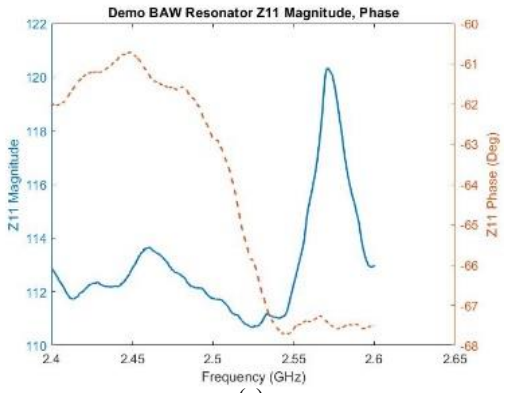
After fabrication, several devices - GHz transducers, FBAR and CMR resonators – were tested to confirm that they work (Fig. 4). Due to poor selectivity of the buffer layer to the oxide sacrificial layer, PMUT device yield was poor and therefore not tested at this point. Using a GSG probe, a 100 µm square GHz transducer was tested in pulse-echo mode by applying a 50 ns, 2.55 GHz, 3.5V amplitude RF pulse to drive the transducer and measuring the received echoes from the same transducer with a high-frequency oscilloscope. The amplitude of the first acoustic echo was measured to be >80mVpp amplitude through a 3dB attenuator (Fig 5a), and is comparable to previously reported echo amplitudes (albeit with different thin film stacks). Resonators were tested by using a network analyzer (ENA 5061) to measure impedance and S-parameters of device resonances (Fig 5b). Due to how signal and ground pads are on different metal layers (top electrode and bottom electrode, respectively) with no vias connecting the layers, de-embedding shorts were difficult to realize and therefore the resonator structures were not de-embedded – hence measured resonances will have relatively low quality factors due to parasitic loading from pads (100 µm by 200 µm). The FBAR resonator was a simple square shape of 150 µm x 150 µm dimension. Release holes were placed within the structure due to the timed etch. The tested CMR device was designed with 5.54 µm pitch and 170 µm long fingers, with 4 finger pairs. The FBAR and CMR resonance frequencies matched the design frequencies of 2.5 GHz and 800 MHz, as shown in Fig. 5(b) and 5(c).



(a)



(b)



(c)

Figure 5. Device measurements: (a) Receive signal for 100 µm GHz BAW transducer, (b) CMR S11 measurement, (c) 100 µm FBAR Z11 measurement.

CONCLUSIONS AND DISCUSSION

This work has successfully demonstrated the feasibility of integrating both bulk-coupled GHz ultrasonic transducer devices and resonator CMR and FBAR type devices on the same process flow. Several fabrication issues remain to be addressed such as the top SiN layer getting etched in the vapor HF release process, and unoptimized stress in the released AlN films. The process flow has the potential to enable a wide variety of MEMS devices by changing the thickness of two layers, namely the buffer and the piezoelectric layer.

In addition, in this iteration, the process flow was kept simple as a proof of concept to show that different Piezo-MEMS devices

can be fabricated using the same process flow. Several important features need to be added to the process flow to make it suitable for both post-CMOS integration and commercial use. These include 1) a patterned release layer – this allows released devices of different geometries to be more easily fabricated by simplifying the release etch step, 2) vias between top and bottom electrode and between bottom electrode and CMOS metallization – these vias allow the Piezo-MEMS electrodes to connect to the CMOS metal stack, and 3) a trimming step for adjusting resonator resonance frequencies.

Furthermore, to transform this work into a full PDK, several key components, in addition to the final optimized process flow, need to be developed. We envision two versions of the PDK – an initial MEMS only layout PDK and a final MEMS on CMOS PDK. The layout PDK will be implemented for KLayout, due to the free and open-source nature of the software, which enables easy access, and also due to the support for Python scripting and DRC checking. In addition to the necessary files for setting up the software layout environment, it is necessary to also provide reference designs with example FEM models and measured S-parameter data, which is usually not provided with current MEMS PDKs but would give designers increased confidence in their designs. A CMOS-MEMS PDK will need to be implemented in Cadence Virtuoso, as that is the primary software supported by most CMOS foundry PDKs. In addition to the numerous layout environment setup files required for Virtuoso, other components that need to be provided include 1) DRC and LVS rule decks in either Cadence PVS or Siemens Calibre, 2) schematic simulation models and measured S-parameters for reference devices, and 3) layout P-Cells to automatically generate MEMS device layouts. In current PDKs, schematic models are generally not provided due to the amount of work required to develop, however, they are extremely important for CMOS designers to verify that their circuits interact correctly with the MEMS devices.

ACKNOWLEDGEMENTS

The authors would like to acknowledge funding from DARPA SBIR Phase I and Phase II under the MEMS PDK program. Help in process development was instrumental from CNF staff, especially Tom Pennell. This work was performed in part at the Cornell NanoScale Facility, a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (Grant NNCI-2025233).

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