MICROMACHINED THICK-FILM COPPER POWER INDUCTORS AND TRANSFORMERS FOR INTEGRATED POWER CONVERTERS

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ABSTRACT

This work presents surface-micromachined, air-core, power inductors and transformers for next-generation, integrated, high-frequency switching power converters operating in the 50–500 MHz frequency range. The high-performance devices are realized by a multilayer, copper electroforming process that enables low resistance, three-dimensional, free-standing structures for high mutual inductance coupling and low parasitic capacitance. Three fabricated inductor designs are presented with areas 1–4 mm^2, inductance densities > 100 nH/mm^2, and quality factors up to 21. Three transformer designs are also presented, all with areas 2.25 mm^2 and primary inductances of 47 nH but with variable secondary inductances to yield voltage gains from 1:1 up to 1:3.5.

INTRODUCTION

Power converters will have an essential role in empowering mobile microsystems by providing efficient interoperation of various subsystems—batteries, energy harvesters, actuators, and sensors—but must do so within diminishing size and weight constraints [1]. The miniaturization of today's power converters is typically limited by the requirement for high-efficiency passives, e.g. inductors with high quality factors [2], which often entails the use of large external components. Newer conversion architectures have pushed switching frequencies up into the multimegahertz realm and have reduced the passive size requirement [3]. For instance, a 233 MHz buck dc-dc converter has demonstrated 80-87% efficiency utilizing four 4 nH off-chip air-core inductors [2]. However, many magnetic materials exhibit prohibitively large magnetic core losses above several MHz [4], while air-core GHz RF passives typically have inductances and quality factors that are still too low for efficient conversion [2].

In [5] we presented batch-fabricated, micromachined air-core inductors and transformers to bridge this frequency gap with high quality factors and efficiencies in the 100–500 MHz frequency range. The surface-micromachined, multilevel metallization process enabled 10-µm-thick copper windings for low resistance and enabled two-layer stacking of windings for enhanced mutual coupling and higher inductance density. The low temperature of all the processing steps makes it feasible to consider post-CMOS integration of the inductors on silicon power electronic circuits.

We now extend the study of these devices by introducing 1) the patterning of the interlayer dielectric into support posts for reduction of parasitic capacitance, resulting in up to ~20% improvement in quality factors and operating frequencies, and 2) the design of transformers of various turns ratios using the same fabrication process. The image of one such fabricated inductor in Fig. 1 highlights the freestanding, stacked spiral structure that is common to both the inductors and transformers of this work. Each transformer, such as that shown in Fig. 2, is comprised of two air-core inductors with windings that are nested and interleaved for strong mutual magnetic flux coupling. Primary and secondary coils are each stacked for increased inductance densities (>300 nH/mm^2) in voltage-gain configurations. All devices were fabricated on Pyrex substrates for characterization without substrate losses. Planar contact with a 10 Ω-cm silicon wafer is expected to decrease quality factors and efficiencies by 10–20% [5].

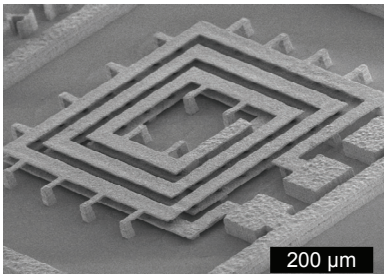


Figure 1: SEM image of a surface-micromachined, stacked, copper spiral inductor.

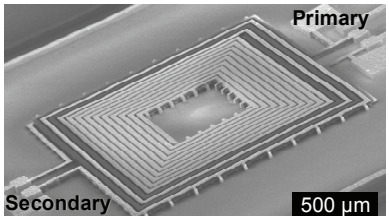


Figure 2: SEM view of a step-up transformer. Secondary winding is charged to display a lighter shade than the dark-shaded primary winding.

DESIGN CONSIDERATIONS

Inductors

The inductors of this work were designed with an emphasis on yielding maximum quality factor, defined as the frequency-dependent ratio of reactance to resistance, $Q = \mathrm{Im}\{Z\}/\mathrm{Re}\{Z\}$. The quality factor of an inductor provides a figure of merit that quantifies the efficiency of magnetic energy storage available to the circuit [6].

In order to roughly optimize inductor geometry, analytic expressions [7] were used to estimate the ratio of dc inductance to resistance, L_{dc}/R_{dc}, which at low frequencies is proportional to Q. From inspection of trends for inductors with ~100 nH and area ~1 mm^2, maximum L_{dc}/R_{dc} was found to occur with a trace width of ~50 µm and with minimum lateral spacing between traces, which for the process presented here was set at 10 µm. With a given fixed outer dimension, L_{dc}/R_{dc} generally increased with the number of inner turns but reached its maximum value in all test cases when the number of turns was ~80% of the space-constrained limit due to the reduced coupling of the smaller inner turns. For this reason, the number of turns was not maximized, and the central 10–20% area of each inductor was left empty.

FastHenry inductance simulation software was used to determine the effect of vertical spacing between upper and lower winding layers on the mutual inductance of the inductors. Simulations indicated that the inductance asymptotically approached perfect vertical coupling (4x the single layer value) with a gap less than 1% of the outer dimension of the device. The devices of this work—with outer dimensions ≥ 1 mm—therefore used an interlayer spacing of 10 µm since a shorter gap would not significantly improve the inductance of the devices but would detrimentally increase parasitic capacitance.

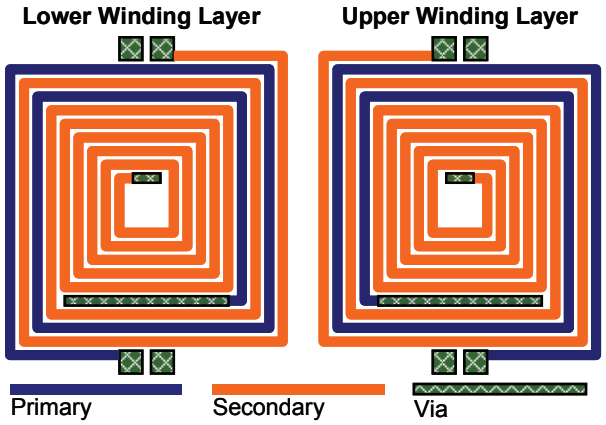


Figure 3: Layout of step-up transformer showing interleaved and nested wiring of primary and secondary coils for mutual coupling.

Transformers

The design of the transformers was primarily focused on enabling a non-unity turns ratio, which required maximizing inductance density. Since a turns ratio of $1:n$ requires an inductance ratio of $L_2 = n^2 L_1$, the maximum achievable turns ratio can be severely limited by size constraints if some minimum primary side inductance is required. A narrower trace width of 30 µm was chosen to allow more turns and to increase the inductance density of these transformers compared to the inductors at the expense of greater dc resistance.

The transformer layout—shown in Fig. 3 for a step-up transformer—employed a hybrid winding scheme in which the outer two turns of the primary and the secondary were interleaved on both the upper and lower winding layers while the remainder of the secondary was nested in the inner turns. This arrangement allowed transformers with non-unity turns ratios to leverage the strong vertical magnetic flux coupling for increased primary, secondary, and mutual inductances. The turns ratio was set by the number of inner turns. A unity-gain isolation transformer was obtained by omitting any inner turns; a 1:2.5 ratio was obtained with five inner secondary turns on each of the two layers; and a 1:3.5 ratio was obtained with nine inner secondary turns per layer.

FABRICATION

The devices were fabricated on Pyrex wafers using a thick-film copper electroforming process capable of producing three-dimensional structures. This process consisted of two stages: 1) the layer-by-layer building up of the structure by consecutively electroplating copper through 10-µm-thick, patterned photoresist molds, as in Figs. 4a & 4b; and 2) the release of the structure by removal of the photoresist molds and seed layers, as in Fig. 4c.

While much of the photoresist mold was removed as sacrificial material during the release stage, the use of photoresist developer as the etchant enabled portions of the mold to remain as structural elements in the final, released devices. This photoresist was used to physically and electrically separate the upper from the lower winding layers. Compared to the continuous interlayer photoresist used previously in [5] (Fig. 5a), the devices in this work featured patterned photoresist support posts (Fig. 5b) for decreased parasitic capacitance. The posts were placed 40–100 µm apart with 20 µm × 20 µm footprints, corresponding to approximately 90% removal of the interlayer photoresist.

In building up each layer, as illustrated in Fig. 4a, AZ9245 positive-tone photoresist was spun and patterned over a thin, sputtered copper seed to create an electroplating mold. After

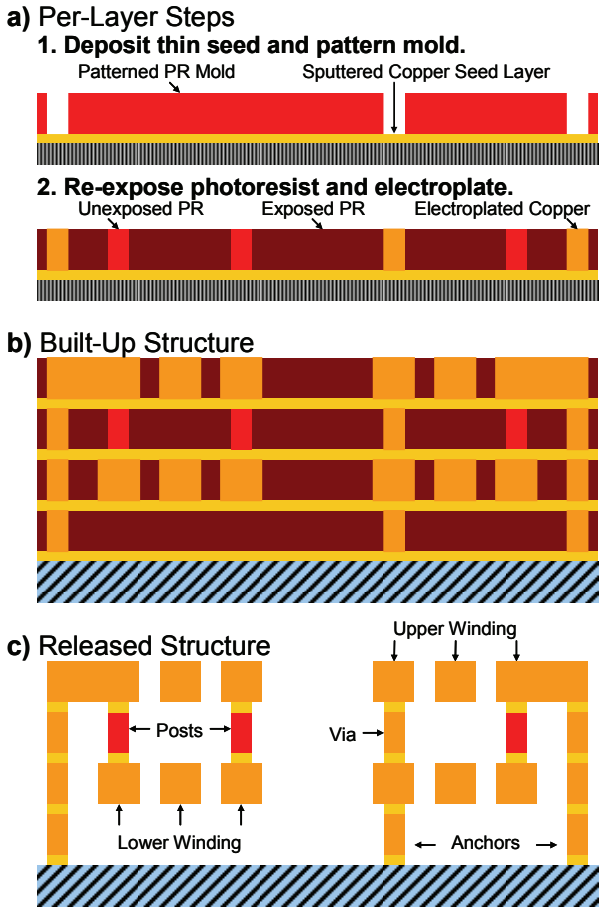
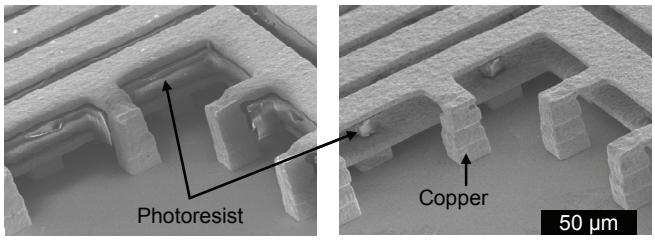


Figure 4: Fabrication process consisting of a) electroplating copper through photoresist molds to construct each layer of b) the four-layer built-up structure, c) which is then released in alternations of photoresist developer and copper etchant.

patterning, the mold was UV-exposed a second time with the support post areas masked from exposure. The mold was then filled with copper using timed electroplating in a copper sulfate bath. These molding and electroplating steps were repeated four times to obtain a layered structure, depicted in Fig. 4b, with each successive copper seed sputtered directly on top of the previous layer.

In the release stage, the exposed photoresist and copper seed layers were then consecutively removed in AZ 400K KOH-based photoresist developer and copper etchant, respectively. After four etch cycles, the final released structures were obtained as shown in Fig. 4c with two copper winding layers suspended in air above the wafer surface.



a) Continuous photoresist layer *b) Patterned photoresist posts*

Figure 5: SEM images of device scaffolding consisting of copper anchors and photoresist support layers.

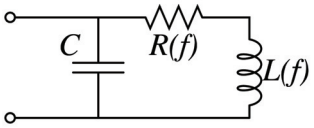


Figure 6: Frequency-dependent inductor model with shunt capacitance.

Table 1: Comparison of circuit-model shunt capacitance with patterned photoresist support posts vs. continuous interlayer photoresist.

Inductor Geometry	Model Shunt Capacitance	
	Continuous Photoresist	*Patterned Posts*
1.00 mm²	0.55 pF	0.39 pF
2.25 mm²	0.90 pF	0.63 pF
4.00 mm²	2.15 pF	1.34 pF

PARASITIC CAPACITANCE MITIGATION

An inductor model was required in this work to quantify the parasitic capacitance of the inductors and to determine the performance improvement associated with the patterning of the interlayer photoresist into support posts. The inductors were modeled by a series *RL* circuit with parallel, shunt capacitance as shown in Fig. 6. Additionally, the *R* and *L* values were functions of frequency, *f*, to account for the effects of eddy current generation within the traces. The resistive and inductive elements maintain their dc values up to a certain frequency f_k, past which the value of the resistive element increases with frequency while that of the inductive element conversely decreases [8]. The frequency-dependence of the resistive elements was found to follow the form,

$$X(f) = X_{dc}\left[1+\left(\frac{f}{f_k}\right)^{s_X}\right]^{o_X}, \qquad (1)$$

with each occurrence of '*X*' replaced by '*L*' or '*R*' for inductive and resistive elements, respectively. The parameters used in Eq. (1) were obtained by a best fit of the model to the data for all three measured inductor designs: f_k=37.7 MHz, s_R=1.24, o_R=0.554, s_L=2.18, and o_L=-0.0225.

The shunt capacitance values were extracted by fitting the circuit model to the measured data both for inductors with support posts and for those with continuous photoresist layers. As listed in Table 1, inductors with patterned support posts exhibited a 27–38% reduction in this parasitic capacitance—with the greatest reduction occurring in the largest-sized inductor. The benefit of parasitic capacitance mitigation is illustrated by the plots of inductor performance measurements in Fig. 7; a 4 mm² inductor having intermittent support posts is shown to have 26% higher self-resonant frequency and 21% higher peak quality factor than another inductor of identical dimensions except having a contiguous photoresist separation layer. All other results presented in this paper are for devices with patterned photoresist posts.

MEASUREMENT AND CHARACTERIZATION

One- and two-port scattering parameters of the inductors and transformers, respectively, were measured through an Agilent E8361A Network Analyzer with frequency sweeps from 10 MHz to 8 GHz. The scattering parameters were then converted to impedance parameters in order to extract the measured inductances, $\mathrm{Im}\{Z\}/2\pi f$, and resistances, $\mathrm{Re}\{Z\}$.

Inductors

The inductance, resistance, and quality factor were measured for each of the inductors. A summary of these performance

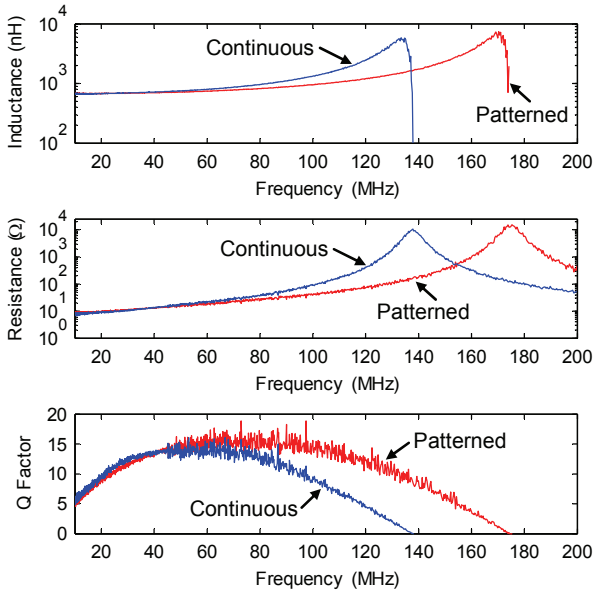


Figure 7: Plots of frequency-dependent performance characteristics of 4 mm² inductors, comparing effect of patterned vs. continuous interlayer photoresist support.

Table 2: Performance comparison of power inductors.

Inductor Comparison	Performance Characteristics					
	Area (mm²)	L_{dc} *(nH)*	*L/Area (nH/mm²)*	Q_{max}	f @ Q_{max} *(MHz)*	R_{dc} *(Ω)*
This work, air	**1.00**	**90**	**90**	**21**	**400**	**1.6**
This work, air	**2.25**	**200**	**89**	**21**	**200**	**3.2**
This work, air	**4.00**	**675**	**169**	**16**	**75**	**8.5**
Park, air [9]	1.69	36	21	44	1200	2.8
Fukuda, NiZn [10]	36	1400	39	40	5	0.67
Wang, NiFe [11]	5.69	160	28	6	4	0.26
Sato, FeCoBN [12]	21.9	370	17	15	7	-

characteristics is found in Table 2 along with results from several other works for comparison. Even without the use of magnetic materials, these inductors have significantly higher (2-8x) inductance densities and operate at higher frequencies than comparable ferromagnetic-core devices [10-12].

Transformers

Although the low-frequency transformer inductances and resistances are readily obtained through the two-port impedance parameters [5], performance characterization requires accounting for the load. For this reason, the measured scattering parameters are transformed into *ABCD* parameters for modeling the effect of attaching a load to the secondary port.

While optimal efficiency can be found using only the measured scattering parameters and the expression for maximum available gain in [13], such calculation does not yield the associated voltage gains and load impedances. The matched load with which the transformer operates at maximum efficiency at each frequency is found as a function of the *ABCD* parameters by solving for Z_L,

$$\left(\overline{A}C+A\overline{C}\right)\overline{Z_L}^{\,2}+\left(\overline{B}C-B\overline{C}+A\overline{D}-\overline{A}D\right)\overline{Z_L}-\left(\overline{B}D+B\overline{D}\right)=0\,. \qquad (2)$$

Efficiency, defined as the real power delivered to the load in proportion to the real power input to the transformer, is then calculated as a function of Z_L:

$$Eff=\frac{\mathrm{Re}\{Z_L\}}{\mathrm{Re}\{(AZ_L+B)\overline{(CZ_L+D)}\}}, \qquad (3)$$

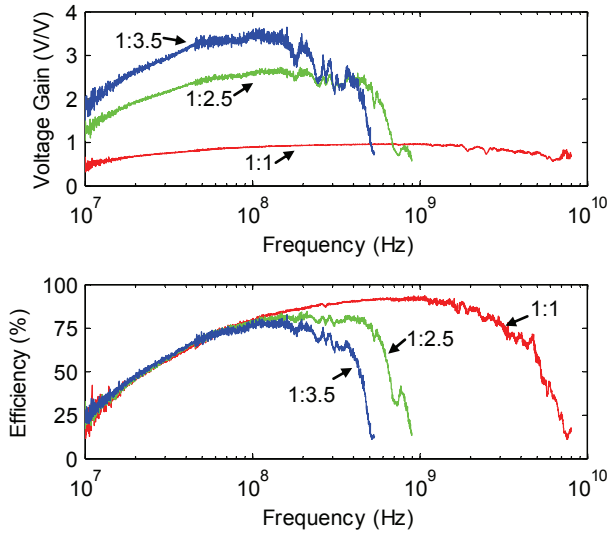


Figure 8: Predicted matched-load performance characteristics of transformers of different turns ratios.

Table 3: Performance comparison of microtransformers.

Transformer Comparison	Performance Characteristics							
	Area (mm^2)	$L_{1,dc}$ (nH)	$R_{1,dc}$ (Ω)	$L_{2,dc}$ (nH)	$R_{2,dc}$ (Ω)	*k*	*Eff (max)*	*Eff (50 Ω)*
This work,air,1:1	**2.25**	**47**	**2.1**	**47**	**2.1**	**0.85**	**91%**	**84%**
This work,air,1:2.5	**2.25**	**47**	**2.1**	**309**	**7.0**	**0.71**	**82%**	**48%**
This work,air,1:3.5	**2.25**	**47**	**2.1**	**492**	**9.0**	**0.62**	**78%**	**35%**
Yamaguchi, air [14]	7.44	70	-	65	-	0.35	67%	-
Kurata,CoFeSiB[15]	1.38	50	-	50	-	0.92	-	54%
Wang, NiFe [16]	23.73	400	0.5	400	0.5	0.93	72%	63%

which is equivalent to the expression in [13] when Z_L satisfies Eq. 2. With Z_L identified the voltage gain of the loaded transformer can be calculated from

$$G_v = \left| \frac{Z_L}{AZ_L + B} \right|. \quad (4)$$

Using the measured *ABCD* parameters and the values of Z_L solved from Eq. 2, the voltage gains and efficiencies of the three transformer designs were plotted in Fig. 8 for the case of maximum efficiency. While voltage gain is approximately equal to the turns ratio for the case of matched loading, it is important to note that significantly higher or lower voltage gains can be attained on the same transformer with different loads. For instance, voltage gains >15 could be obtained from the 1:3.5 transformer with capacitive loads of 1–6 pF, albeit with efficiencies < 10%.

The low-frequency resistances and inductances measured from each of the transformers are summarized in Table 3 along with the maximum efficiencies, both as measured with 50-Ω-loading and as projected from Eqs. 2 and 3 with matched loading. Compared to other air-core transformers [14], the devices here have demonstrated greater inductance densities, coupling coefficients, and efficiencies. Although the coupling coefficients are less, the efficiencies of these are-core transformers are also competitive with those of magnetic film devices [15, 16].

CONCLUSION

The use of thick-film micromachining enabled air-core inductors and transformers with high performance for next-generation switched power conversion architectures operating in the frequency range of 50–500 MHz. Strong vertical mutual coupling provided inductance densities rivaling those of thin-film magnetic devices, while dielectric removal was shown to reduce parasitic capacitance and to increase quality factors and operating frequencies.

ACKNOWLEDGEMENTS

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