BOSCH-DRIE SHAPING MEMS – HISTORY, APPLICATIONS AND FUTURE DIRECTIONS

Franz Laermer[1] and Andrea Urban[2]
[1]Robert Bosch GmbH, Corporate Research Microsystems, Stuttgart, Germany
[2]Robert Bosch GmbH, Engineering Sensor Process Technology, Reutlingen, Germany

ABSTRACT

Deep Reactive Ion Etching (DRIE) is virtually shaping the MEMS-field. The basic technology originally developed at Bosch is free from the design restrictions and compatibility problems related to the old wet-etching technology which was based on potassium hydroxide (KOH-) solution. The technology has enabled a wide range of new devices like the inertial sensors for acceleration and yaw rate detection, pressure sensors for mid- to high-pressure applications, MEMS microphones, micro-mirrors and quite recently also timing devices fabricated in silicon. These products conquered both the automotive application area, and later on also the consumer field. From the surface-near micromachining of the early development stages, DRIE is nowadays heading towards a true 3D-microstructuring. Pressure sensors, microphones and micromirrors represent first examples of this trend, but also packaging applications like DRIE-structured silicon caps, functionalized silicon carrier substrates for intelligent systems-in-package, and through-silicon vias (TSV's) for chip-stacking and new chip-integration concepts are receiving increasing attention.

This paper leads from the early development phase targeting first high-volume products, to the development of advanced high-rate etching solutions targeting today's new and challenging product families.

INTRODUCTION

Precise and reproducible microstructuring technologies are the key to the fabrication of arbitrarily shaped silicon devices, e.g. sensors and actuators. From the very beginning of MEMS, device performance features were closely linked to the limitations of the microstructuring technology, which was at the time mostly wet etching in KOH and other alkaline solutions. This technology was suitable for the fabrication of comparatively simple devices like pressure and mass-flow sensors, where etching of rectangular groves with tilted (111)-sidewalls from the wafer backside was sufficient to produce the required membranes at the wafer frontside, but when it came to more complex geometries, KOH-etching was no longer a good choice. The etching behaviour is selective on crystal orientation, with fast etching crystal planes like (100) or (110), and slowly etching crystal planes like (111) which normally appear as the structural sidewalls. Corner compensation techniques are often required for non-convex geometries, which significantly restrict design flexibility and depend on process time thus reducing process control.

It became obvious that new microstructuring techniques where needed to overcome the design restrictions and the compatibility problems involved with KOH in a semiconductor infrastructure. The capability to produce arbitrarily shaped geometries in silicon was recognized as a true enabler for MEMS devices of enhanced functionality. Plasma etching was already well-established in IC-manufacturing, and it was also well known that plasma was offering enhanced flexibility with regards to etchable geometries. However, low etching speed (<1 µm/min), rapid mask erosion during the etch (selectivities < 15:1), and achievable etching depths of only some µm's made it inapplicable to the MEMS specific needs. A significant enhancement of the existing plasma etching technology to meet the MEMS requirements was achieved by the introduction of the "BOSCH-DRIE" plasma process, which was embraced by the MEMS community as the answer to their long-felt needs.

The "BOSCH-process" provided the high etching-speed and mask selectivities needed at that time (>2µm/min and >100:1, respectively), compatibility to standard photoresist masking, IC technology and IC factory infrastructure, as well as vertical sidewalls and minimum critical dimension loss to ensure good reproducibility and high accuracy of critical devices.

PROCESS TECHNOLOGY

Dependent on process chemistry, etching-speed is closely related to the concentration of radical species or of charged species, the so-called ions, or to both of them. Chlorine or bromine dominated process chemistries do not etch silicon spontaneously at room temperature, at least not at significant rate, for lack of activation energy to keep the etching reaction progressing, and for the need to remove reaction products of low volatility from the wafer surface. The driving factor behind the latter mechanisms is an energetic ion flow to the wafer surface to provide both activation energy and reaction product removal to/from the local etching areas, which requests for large ion concentration or ion density in the plasma as generated e.g. from an ECR-source [1]. Perpendicular directionality of the ion impact onto the wafer surface is the source of anisotropy of the etch, since ions preferentially hit the bottom compared to the sidewalls of a trench. As a consequence, the bottom of a trench etches much faster than the sidewalls in this case. In addition to the intrinsically anisotropic characteristics of a chlorine or bromine etching chemistry, sidewall passivation may be added by deposited sidewall films on a molecular scale, or by oxidation or nitrification of the sidewall surfaces on an atomic scale to improve or tailor profile accuracy and evolution. With ion-impact being the rate-limiting factor, massive ion energy flow is needed to achieve an increase in etch-rate. The latter however accelerates mask material erosion as well. As a general tradeoff, selectivity and critical dimension control are diminishing with a more aggressive ion bombardment for higher etch-rate. This is typical for a situation of an ion-induced etching reaction.

In contrast to the halogens of lower reactivity like chlorine and bromine, fluorine-based chemistry is characterized by an immediate and spontaneous reaction of the fluorine radicals with silicon atoms, once absorbed onto the silicon surface. The reaction products are silicon fluorides, predominantly SiF_4, which shows a high volatility and readily leaves the surface without further assistance. At room temperature, no activation energy beyond thermal energies is needed to induce the reaction which is a purely chemical etch. Yielding highly volatile reaction products, no removal mechanism is required to clear the etch bottom from reaction products at room temperature. As a consequence, application of an energetic ion flow to the surface is generally not creating anisotropy of the etch profiles nor accelerating the etching speed significantly. Etching proceeds at any unprotected silicon surface with no preferential orientation, making the etching

profiles highly isotropic. As a particular advantage of the purely chemical etching nature of the fluorine radicals, selectivities may reach extremely high values, and photoresist masking is feasible. Etching speed scales with the amount of fluorine radicals reaching the silicon surface, which requests for a large density of chemically active species rather than ions generated in the plasma. Higher etching-speed from larger fluorine radical concentration levels is not conflicting with photomask stability, as long as the wafer temperature is maintained within certain borders (<100°C).

In MEMS-applications, high anisotropy is a must and directionality needs to be introduced somehow into the etch, except for sacrificial release processes where lateral underetching of fabricated structures is on target and isotropy is welcome. In principle, several options exist to reach anisotropic etching behaviour:

1. Ion-induced reaction mechanism
2. Non-volatile reaction products, which need ion-assistance to clear them off the surface
3. Sidewall passivation by reaction of additives with silicon on an atomic level
4. Sidewall passivation by deposition of thin films on a molecular level

Option 1 is the situation typical for chlorine and bromine based chemistries, see e.g. [1]. It is not applicable to fluorine chemistry (see comparison in [2]).

Option 2 is contributing to the anisotropy of chlorine and bromine etches (together with option 1). It also contributes to the anisotropy of fluorine-based etches at cryogenic temperatures (-100°C and below) [3].

Option 3 is in principle applicable to all halogen chemistries and consists of silicon surface oxidation or nitrification by the appropriate additives like oxygen, nitrogen and/or nitrous oxides. For chlorine and bromine chemistries, this option is often used in combination with 1 to tailor profile details. For fluorine chemistry, this option is relevant for most of the anisotropy observed in cryogenic dry etching (see above), and for the anisotropy achieved in the so-called "black silicon method" [4] at room-temperature. At room-temperature, sufficient stability of the protective layer on the sidewall surface is achieved only for a large excess of the additive gas compared to the fluorine supply gas (sulfur hexafluoride, SF_6) which is at the cost of etching-speed. At cryogenic temperature, stability of sidewall passivation is increasing and additive gas flow can be reduced to levels more economic with regards to etching-rate [5].

Option 4 is applicable to all halogen chemistries. In older chlorine or bromine based etches, using chlorocarbons (eg. CCl_4), chlorofluorocarbons (CCl_2F_2), bromocarbons (CBr_4), bromofluoro-carbons (CF_3Br) or bromochlorocarbons (CCl_2Br_2) as halogen supply gases, sidewall polymer films were building up from the monomers left behind after splitting off a halogen radical as an etching species. For fluorine chemistries, fluorocarbons (CF_4, C_2F_6, CHF_3, C_4F_{10}, C_4F_8) also split in the plasma into fluorine radicals and remaining monomers, which may or may not build-up polymeric sidewall protective films depending on the amount of excess fluorine. The more excess fluorine available, the faster the achievable etching speed (which depends on free fluorine radical concentration), however the lower the tendency to build up a protective sidewall film. In addition, recombination between fluorine radicals and unsaturated monomers eliminates active species pairwise, and competes with etching silicon and protective sidewall polymer buildup, repectively. This makes a "mixed process" consisting of fluorine delivering and polymer forming compounds like mixtures of SF_6 and C_4F_8 both inefficient and difficult to control.

The "Bosch process" overcomes these limitations by generating a high-density plasma remote and decoupled from the wafer combined with a sophisticated etching and passivation scheme, and a low energetic ion impact onto the wafer. Etch and passivation steps are alternating each other separated in the time domain and are controlled independently from each other [6].

During the etching steps, sulfur hexafluoride (SF_6) readily delivers fluorine radicals after excitation of gas molecules by electron impact from the plasma. During the passivation steps, an unsaturated fluorocarbon gas is excited in the plasma to generate polymer-forming monomers which build up teflon-like protective sidewall films. From a number of potentially suitable fluorocarbons, octafluorocyclobutane (C_4F_8) was found to be the best choice.

The discontinuous nature of the process overcomes a number of general problems involved with anisotropic etching: pairwise extinction of etching fluorine radicals and passivating polymer-forming monomers by gas-phase recombination is avoided by separating them in the time-domain. This is of particular importance for the plasma source area itself where high concentration levels of both species are generated and the recombination losses would be strong. Outside the source area, in a more diluted state, the situation is less critical. It was shown by the authors that if separation is maintained mainly for the plasma source, process performance still remains high even with species mixing below the plasma source in the downstream area under conditions of so-called ultrafast gas-pulsing [7].

The nature of the passivating teflon-like polymer requires only low-energetic ion impact during the subsequent etching step for its complete removal from the etching floor. For the low ion energies needed, photoresist and SiO_2-mask erosion remains very small yielding the high selectivity values needed from the application side.

As a side-effect resulting from the sequence of etching and passivation steps, some sidewall scalloping occurs typically on the order of some 10 nm's. Although undesired in some applications e.g. in the optical domain, sidewall scalloping reduces the risk of silicon spikes formation on the trench floor. In any plasma process of high anisotropy and selectivity, particles or residues of all kind act as micromasks which may yield corresponding silicon patterns if they endure etching long enough. In the "Bosch-process", micromasks smaller than the scallop-sizes are undercut and extinguished from the surface before leaving their imprint in the silicon. Only if their size is exceeding a critical dimension limit beyond what the process can tolerate (undercut), they will cause undesired patterns on the trench floor.

EQUIPMENT TECHNOLOGY

From the etch-rate target of several µm/min, it is clear that a high-density plasma source with species densities on the order of $10^{12}…10^{14}$ cm^{-3} in the plasma generation zone is needed to meet the challenge. In addition, in a pressure regime of several Pa (Pascal) it is easier to reach the required densities of chemically active species, however requesting the plasma source to remain in a high-density plasma mode. In 1990, the only high-density high-pressure plasma source available was the microwave surfatron at 2.45 GHz excitation frequency [8], [9]. Later on, inductively coupled plasma (ICP) sources made their way into the equipment industry, most of them powered at 13.56 MHz radio frequency. Both types of sources show astonishingly similar key performance features. Should plasma source power levels in future exceed 5 kWatts for the extremely high etch-rate conditions, the question

may be raised again whether the microwave magnetron-powered or the RF-powered plasma source is the better option on a longer term. Microwave technology enables virtually unlimited power levels at a very low cost, for reasons of the high-volume production of magnetrons for industrial and commercial heating applications which is driving down prices per kWatt output power to very low levels. In addition, microwave equipment with waveguides, tuning studs, circulator, beam splitters and water load can bear practically any reflected power levels without suffering damage or instability of plasma operation. These facts make it worthwhile to keep a close eye on this potential alternative to the inductively coupled plasma sources as of today. The microwave surfatron or similar constructions may potentially come back in the form of "plasma boosters" upstream of an ICP-source, to generate just huge amounts of neutral radicals in a "chemical reactor", with the ICP source below adding a homogeneous ion distribution of low-temperature and low-plasma potential to provide directionality in the etching reaction [10].

Today's dominating plasma source in the equipment industry is the inductively coupled plasma (ICP-)source. The following schematic diagrams are showing three types of ICP-sources: The first one (Fig. 1) which is sometimes also called "transformer coupled plasma" (TCP) is using a planar coil on top of a dielectric window for generation of the plasma. Plasma generation is at relatively close distance to the wafer, which limits applicable power levels (and achievable etching-rates) in a "Bosch"-type process: for power levels above 1 kWatt, hot electrons from the dense plasma are causing etch profile distortions which are correlated with the soft sidewall passivation film. The advantage of this configuration is the uniform plasma potential and charge distribution over the wafer surface, which keeps asymmetric tilting of etched sidewalls extremely small. For the fabrication of micromachined gyroscopes with out-of-plane mode for the detection of Coriolis forces, this is highly beneficial for the reduction of cross-coupling between base vibration mode and detection mode (see later in this paper).

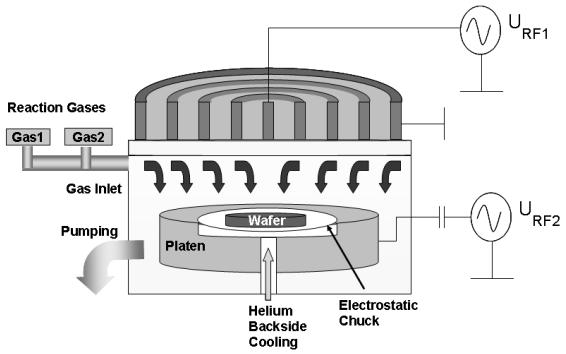

Fig. 1: Inductively coupled plasma source with planar RF coil for uniform excitation of the plasma. He-gas serves for cooling the wafer, a second RF generator is biasing the substrate electrode for accelerating ions from the plasma towards the wafer.

The second type of inductive source (Fig. 2) is using a RF coil wound around a dielectric vessel. The plasma is excited inside the vessel, where chemically active species and ions are generated at a high density. This is the classical ICP configuration. Plasma excitation is non-uniform, with denser plasma regions close to the driving coil near the dielectric wall, whilst plasma excitation towards the center of the reactor is comparatively weak, following the magnetic field distribution created by the inductive coil (compare Biot-Savart's-equation for field distribution calculation). The drawback is that process gas flowing through the center of the vessel is excited only comparatively weakly, and large amounts of more or less unexcited process gas are diluting the active species created in the boundary area, which is at the cost of overall rate. Either the reactor vessel is designed for "small diameter" (equivalent to high surface-to-volume ratio) to direct most of the process gas through high-density areas near the dielectric walls, or as an alternative, liners etc. are introduced into the reactor center to prevent process gases from flowing through the areas of only weak excitation. In general, in an ICP-tool the wafer is more remote from the plasma excitation zone. The diffusion or drift zone between plasma generation and substrate position allows the plasma to cool down efficiently before reaching the wafer, which enables also high plasma power levels on the order of 3…5 kWatts. As a major drawback, plasma potential and ion current distribution are less uniform, yielding asymmetric tilting of etched sidewall profiles (outer sidewalls of etched structures show more negative slopes than inner sidewalls) which has a negative impact on the performance e.g. for gyroscopes with out-of-plane detection mode.

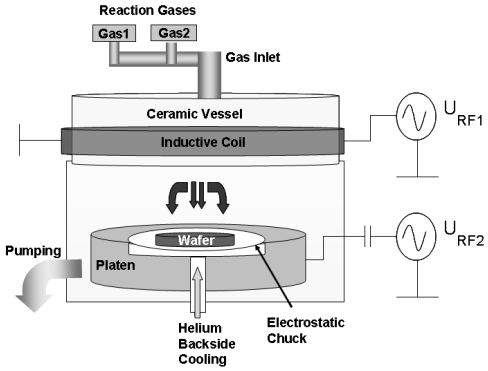

Fig. 2: Classical ICP-tool with inductive coil wound around dielectric vessel. The wafer is located downstream from the source, separated by a drift zone for plasma cooling and homogenization of species distribution.

A solution to overcome this drawback is depicted in Fig.3: A magnetic ion collimator is placed between the plasma source exit and the wafer position. Some magnetic enhancement of the plasma discharge itself takes place, boosting the source efficiency to some extent. Most importantly, magnetic fields of opposing signs counter-act as lenses acting onto the charged particles which are drifting down from the source region towards the wafer, tailoring spatial plasma potential and ion current distributions [11].

As the one alternative, uniformity of the plasma potential distribution in the sheath close to the wafer location can be targeted for optimization. With a proper adjustment of the DC currents to the magnetic coils for best plasma sheath potential homogeneity, profile tilting can be reduced to the low levels as compared to the configuration shown in Fig. 1, yielding similarly high performance for the types of gyroscopes with out-of-plane detection mode regarding undesired mode coupling (see below).

Uniformity of etching depth is another matter of increasing concern for growing wafer sizes, e.g. from 6" to 8" diameter. A typical phenomenon on etched wafers is a rate increase from wafer center to edge, the problem getting the more severe the larger the wafer sizes. One of the reasons for higher etching speed at the

wafer border compared to the wafer center is an enhancement of etching species concentration because there is no more silicon consuming the fluorine radicals outside of the wafer boundaries. This phenomenon might potentially be compensated by placing a "dummy-load" in the form of a silicon or carbon absorber ring of appropriate width around the wafer. Absorber solutions like that are not appreciated in a manufacturing environment, since they are non-adjustable (except by changing their geometries), reduce the overall etching-rates, and introduce a consumable to the reactor design which represents a serious particle source as well.

An additional reason for the rate increase from wafer center to edge is an enhancement of the ion current drawn to the wafer boundaries as compared to the wafer center: the dielectric surface of the substrate electrode surrounding the wafer area is less attractive to charges from the plasma sheath than the wafer itself, the latter having a more direct connection to the biasing radio-frequency power and a lower impedance towards the plasma. The attempt to reach impedance matching between the wafer and its surroundings by introducing e.g. a metal or a conductive layer covered by a tailored dielectric shield again leads to an optimization problem for mechanical parameters like geometries and layer thicknesses, which is not appreciated as a good manufacturing solution either.

The second alternative to make use of the magnetic collimator depicted in Fig. 3 is for optimizing its spatial filtering characteristics to the charged particles on their way to the wafer for targeting a best-as-possible etch-rate distribution. Adjusting the currents through the collimating electromagnets to redirect ion flow away from the wafer border areas and focus more towards the wafer center can be applied to compensate the rate increase from center to edge and to achieve an optimized etch-rate uniformity. Etch-rate variation of +/- 1% (min-max) is possible for an open silicon area of 20 % on a 6"-wafer, which represents a typical silicon load situation in MEMS. Note that the optimized collimator adjustments for best profile uniformity (smallest asymmetric profile "tilting") are in general significantly different from those for best etch-rate uniformity. This trade-off between different optimization targets requires compromising with respect to the individual application, to focus on optimizing its most critical specification parameters and give away on others.

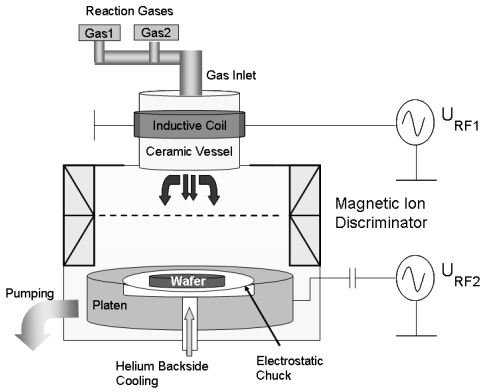

Fig. 3: ICP-source with adjustable magnetic ion collimator for homogenization of profile forms over the wafer, or alternatively, for optimized uniformity of the etch-rate distribution over the wafer.

The notching phenomenon well-known for high-aspect ratio trenches is more predominant for the high-density inductively coupled plasma as compared to the low-density RIE conditions, with ion densities being typically by 2-3 orders of magnitude higher than for the RIE sources. Notching appears as a consequence of charging in high-aspect ratio trenches, when the etch reaches a dielectric interface and overetching takes place [12], [13], [14]. Positive ions (kations) accumulate at the dielectric trench floor, and strong electrical fields build up between the floor and the sidewalls of the trench. As a consequence, incoming kations are re-directed towards the sidewalls, away from the positive charges already trapped at the trench floor. Notches cut deeply into the structures where re-directed ions are bombarding the sidewalls. Uncontrolled sidewall attack corrupts mechanical properties of functional devices and represents a serious reliability problem, and a particle source in manufacturing, which makes this phenomenon highly undesirable. Since electrical charges are at the origin of notching, reduction of charging is the key to its elimination.

An advanced pulsing scheme involving both the substrate bias power [15] and the plasma source power [16] yields efficient discharge and notch suppression capabilities, even under strong overetch conditions.

As long as the substrate is powered, negative DC-bias effectively repels negative ions (anions), and only positive ions (kations) and electrons are able to reach the wafer. Since electrons have only little directionality and can be easily deflected, they reach the wafer surface but hardly make it to the dielectric bottom of high-aspect ratio trenches: for discharging their dielectric floors, electrons are inefficient candidates. During phases with bias power off, the substrate looses its repulsive character towards negative ions (anions) which can then reach the wafer surface. Due to their higher mass and directionality, anions are well appropriate for effectively neutralizing accumulations of positive charges even in high-aspect ratio trenches. As an additional effort to increase available amounts of anions, the plasma source power is pulsed together with substrate bias pulsing, switching off the plasma discharge periodically. At each plasma shutdown, during afterglow phases, strong anion peaks are generated. Pulsing frequencies are on the order of 60-100 Hz and several kHz for the substrate electrode and for the plasma source power, respectively.

ENABLING NEW SENSOR DEVICES

In the following section, some sensor devices introduced to the MEMS field by Bosch are discussed. The first product development was for a surface-micromachined capacitive type accelerometer for automotive applications, see Fig. 4. The sensor is fabricated from a 10 µm thick epitaxial polysilicon layer on top of a sacrificial oxide, with a thin buried polysilicon layer underneath used for electrical interconnections [17].

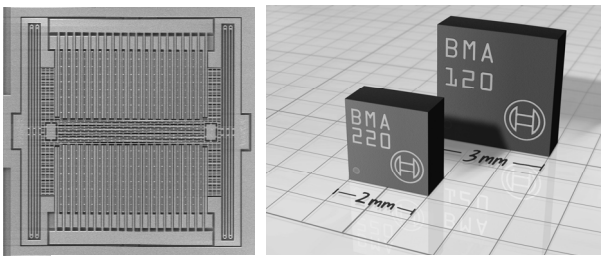

*Fig 4: Single-axis acceleration sensor made from 10 µm thick epitaxially deposited polysilicon by "Bosch-DRIE"(left). The world's smallest triaxial acceleration sensor in 2*2*1 mm^3 package size (right) launched recently as a product.*

High aspect-ratio comb capacitors serve to detect deflections of the seismic mass in response to acceleration. The comb capacitor area is where the anti-notching capabilities of the plasma etching process come into play to assure quality of the safety-critical devices. A first product was introduced to the automotive market in early 1997 for passenger retention systems like the airbag. Later on, follow-up generations of different types of accelerometers for low-g as well as multi-axial sensitivity were brought to the market. Starting from 2004, also the consumer area has been addressed by low-cost and strongly miniaturized triaxial acceleration sensors. Quite recently, Bosch started supplying the world's smallest triaxial accelerometers mainly for cell-phone applications, with a package size of only 2*2*1 mm^3.

After a first generation of gyroscopes [18] fabricated from bulk- and surface-micromachining, a surface-micromachined gyroscope [19], [20] was launched in year 2000 mainly for car navigation and roll-over protection systems, see Fig. 5. This sensor consists of a pseudo-vibrating structure in a rotary oscillation mode, driven electrostatically through high-aspect ratio comb structures. Angular rotation around an axis in the chip-plane yields a periodic out-of-plane torsional vibration of the oscillating mass, as a reaction to Coriolis forces, which is detected capacitively by capacitor plates made from the thin buried polysilicon layer underneath the structure. The measured signal amplitude is proportional to applied angular rate. Profile control of the tether beams carrying the vibrational structure is crucial: any profile deviations from vertical (in particular "asymmetric profile tilting"), give rise to unwanted mode coupling between planar base vibration and out-of-plane detection modes: the so-called "quadrature" component is a serious performance-limiting factor in all gyroscopes sharing a configuration of a planar base vibration mode and an out-of-plane detection mode. Here the considerations described before for tailoring a homogeneous plasma potential distribution over the sheath close to the wafer are of a high relevance to key performance features of the gyroscope.

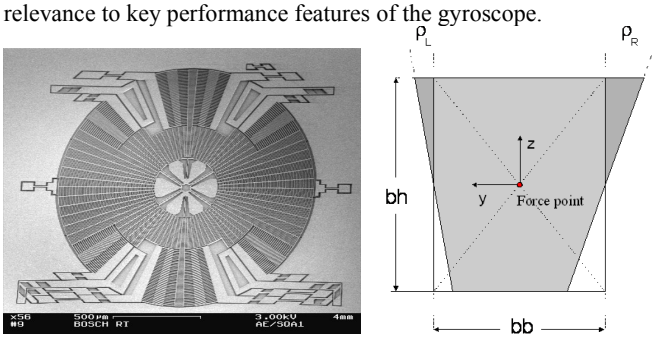

Fig.5: Surface-Micromachined Gyroscope of the rotational type (left). Profile asymmetries ("asymmetric tilting", right) yield undesired mode-coupling and must be avoided.

In 2005, a new generation of surface-micromachined gyroscopes of the linear-linear vibrating type was launched for automotive anti-skidding systems (electronic stability program, ESP), see Fig. 6. One motion mode is excited into a periodic linear vibration by electrostatic forces from a comb-drive, with an orthogonal linear motion mode used for detection of Coriolis-forces resulting from angular velocity. With both orthogonal modes used for drive and detect being planar modes, and detection performed by a second set of comb capacitors, the sensitivity axis for angular rotation is out-of-plane [21]. With the detection mode being chosen as an out-of-plane vibration mode, also in-plane angular rotation speed is detectable by polysilicon capacitor plates underneath the structures. Again, for the latter configuration, mode-coupling between in-plane and out-of-plane vibration modes is a performance-limiting factor. Asymmetric profile tilting as the major cause for the "quadrature" component must be avoided by providing a homogeneous plasma sheath potential distribution over the wafer. Aside from automotive applications in car safety systems, surface-micromachined gyroscopes are receiving increasing attention also from the consumer side, e.g. for image-stabilization in digital cameras. Combining devices with different detection modes and sensitivity axis into a single chip enables multi-sensors for triaxial yaw rate detection, similar to the accelerometer case. Potential applications for multiaxial yaw rate sensors are navigation systems in handheld devices.

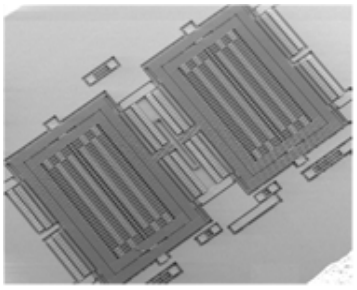

Fig. 6: Surface-micromachined Gyroscope of the linear type. Combining several devices of different sensitivity axis into a multi-chip yields multiaxial (triaxial) yaw rate sensors.

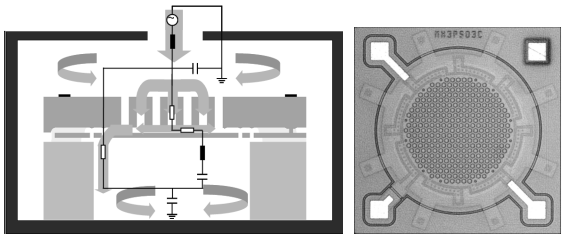

Fig. 7: Schematic cross-section of a MEMS microphone illustrating a reduced network model for electromechanical simulation (left), and an IR transmission picture from the top of the microphone chip (right).

New applications in the consumer electronics field which depend on through-wafer etches are MEMS-microphones, MEMS micromirrors for picoprojectors and the through-silicon-vias (TSV's) for area-saving chip-stacking and bare-die mounting technologies.

For fabrication of MEMS-microphones, a cavern must be etched through the whole wafer thickness to provide the acoustic volume – or sound access-hole – to the sound-pressure sensitive membrane. In addition, the counter-electrode to the membrane-capacitor needs perforation or "vent-holes" to adjust for the correct damping of the acoustic membrane. Fig. 7 shows a schematic cross-section of a MEMS microphone developed at Bosch [22], including a reduced network model for description of its electromechanical behavior, and a picture of the microphone chip itself taken by infrared microscopy from the top. The IR-magnification shows the perforated frontplate, the membrane and its fixation by tether beams underneath the frontplate, and the electrical contact pads. The fabrication technology is the same established process as used for the production of the inertial sensors, with through-wafer backside trenching added for

generation of the acoustic cavity. Particular requirements for the DRIE through-wafer etching step are high-etching speed on the order of 10 µm/min or higher to keep process time reasonably short and within economic limits, and good uniformity of the etching speed over the wafer to keep performance parameters within tight specifications.

Fig 8a and 8b illustrate a schematic process flow for TSV contacts fabrication to an integrated pressure sensor of Advanced Porous Silicon Micromachining-technology (APSM, see [23], [24]). TSV's are etched into the silicon and covered by a dielectric insulation layer deposited to the sidewalls. After opening the dielectric bottom to the metal 1 contact layer of the frontside circuit, the TSV's are either filled with copper by electroplating, or a thin-film metal is conformally coated onto the sidewalls. Contact areas are structured subsequently on the wafer backside. Chips like that can either be directly soldered onto PCB's as bare dice, or stacked on top of other electronic chips, like microcontrollers, multiplexers, memories or RFID for minimum area consumption.

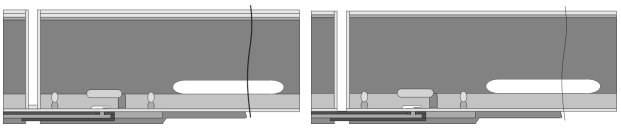

Fig 8a: Process flow for fabrication of TSV's: High aspect ratio trenches are etched and passivated by insulating dielectrics (left). The bottom oxide is opened to metal 1 contacts of the IC (right).

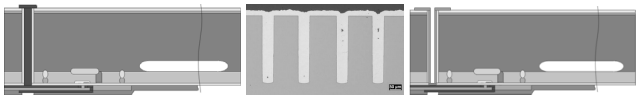

Fig 8b: Trenches with insulated sidewalls are refilled with copper by electroplating (left scheme, and cross-section through refilled test-structures in the middle), or sputter-coated with a metal thin-film, and the metal structured into backside contacts for chip-stacking and bare-die mounting (right scheme).

For etching the deep silicon vias, parameter ramping is often a good choice to use for adapting the process to the increasing aspect ratio of the vias with process progress [25]. This enables a good control of profile evolution, with regards to the needs for subsequent conformal coating and refill of the trenches.

SUMMARY

The "Bosch process" is enabling new micromachining processes and MEMS designs for enhanced device functionalities [26]. Today DRIE is mature technology: pull from the application side has replaced technology push. A lot of development work is still invested from equipment suppliers into improving etch-rate, mask-selectivity, profile control and uniformity as well as suppression of notching for ever higher aspect ratios, both targeting hardware and process. Applications are defining their specific needs and DRIE has to fulfill the individual device specifications. Driven by new applications and the innovation pace from the consumer electronics area, "Bosch-DRIE" technology will continue shaping MEMS into the future.

CONTACT

Franz Laermer
Robert Bosch GmbH, P.O. BOX 106050, DE-70049 Stuttgart
Tel: +49-711-811-7671, franz.laermer@de.bosch.com

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