LOW VOLTAGE COMPLEMENTARY MEMS LOGIC USING PIEZOELECTRIC ACTUATORS

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ABSTRACT

Microelectromechanical systems (MEMS) based on piezoelectric thin films continue to be examined for a variety of versatile sensors and actuators [1,2] The most promising piezoelectric material for actuators is lead zirconate titanate (PZT) because of its large piezoelectric coefficient relative to other piezoelectric thin films such as aluminum nitride and zinc oxide [1]. One drawback of using PZT based MEMS is the difficulty associated with integrating PZT with CMOS to enable embedded control with MEMS components. This paper presents results on using piezoelectrically-actuated MEMS switches for simple logic circuits.

INTRODUCTION

Rather than combining PZT based MEMS with CMOS to enable an on-chip control logic integrated with the MEMS components, one approach is to integrate MEMS logic components within the same process as PZT based MEMS actuators and sensors. Instead of using electronic logic, this approach relies on using mechanical switching elements configured to create the necessary logic components. Lee et. al. successfully demonstrated the concept of MEMS logic components fabricated using the polymumps fabrication process.[3,4] Leveraging this past work, we have developed complementary MEMS logic (CML) components based on the Army Research Laboratory's PZT MEMS fabrication process. The ARL process has previously been used to develop RF MEMS switches capable of operating as low as 2 volts.[5,6] Using the same process flow, PZT mechanical switches configured for optimal operation at DC have been designed and integrated to demonstrate several logic elements.

CONCEPT

The previously reported PZT switch fabrication process created normally open switches by stress engineering the PZT actuator to possess a negative curvature after fabrication. In its simplest form, an inverter requires both normally open (NO) and normally closed (NC) mechanical switching components (see Figure 1). A normally closed PZT switch was designed such that the DC contact cantilever comprised of gold was anchored to the end of the actuator. As the actuator deforms into the wafer plane, the gold cantilever contacts the DC control lines completing the electrical circuit (see Figure 2). The inverter operates as follows. When the input is low (typically 0V) the NC actuator is in contact and the actuation voltage (V_{act}) is presented to the output, which can then be used to actuate the next logic gate. When the input is high (V_{act}) the NC switch opens up and the normally open (NO) switch is closed presenting ground to the output.

RESULTS

The inverter shown in Figure 2 has demonstrated operation as low as 1 V_{DC} (see Figure 3). Successful inversion is illustrated by the output waveform (blue trace) of the inverter always being in the opposite state of the input waveform (red trace) (see Figure 3),. The current version of the CML inverter has a length of 125 µm with a fundamental resonance frequency of approximately 38 kHz. Shorter, faster devices designed within the design tolerances of the current fabrication process are being investigated for improved performance and a reduction in scale. Alternative fabrication processes including the use of sub-micron lithography and electron beam lithography are being investigated as a means to enable nanoelectromechancial (NEMS) logic.

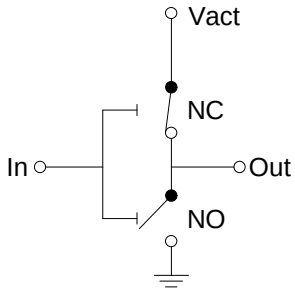

Figure 1: Schematic description of a CML inverter based on using normally closed (NC) and normally open (NO) mechanical switches.

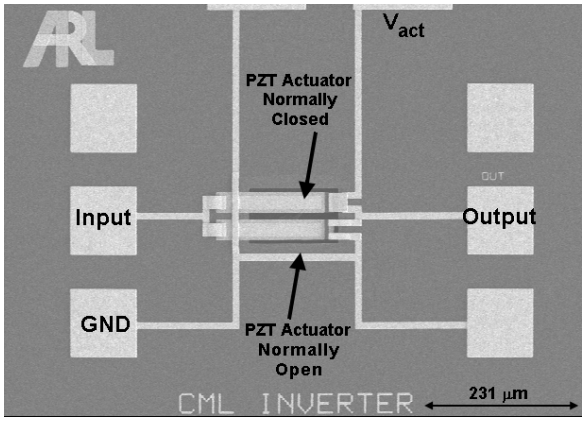

Figure 2: SEM image of a PZT inverter with a normally closed and a normally open switch.

These inverters have exhibited lifetimes in excess of 10^6 cycles (see Figure 4). Referring to Figure 4, a digital voltmeter was used to measure the RMS voltage on the output of the inverter, and a computer logged the time and cycle count. When the device fails open the RMS voltage jumps to V_{act}, and if the device fails closed the RMS voltage goes to zero. The plot shows that some intermittent high resistance failures occurred before the stuck closed failure at around 20 million cycles. The typical failure for these types of devices is due to high contact resistance. This failure mechanism is likely related to contact contamination either from residual organics from the processing or frictional polymers generated during contact, although this is still an area of investigation.

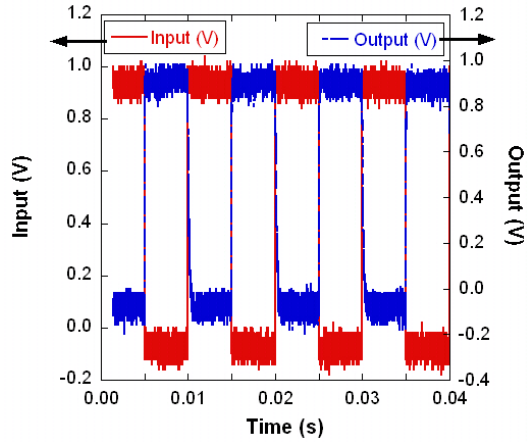

Figure 3: Experimental operation of a one volt PZT based CML inverter.

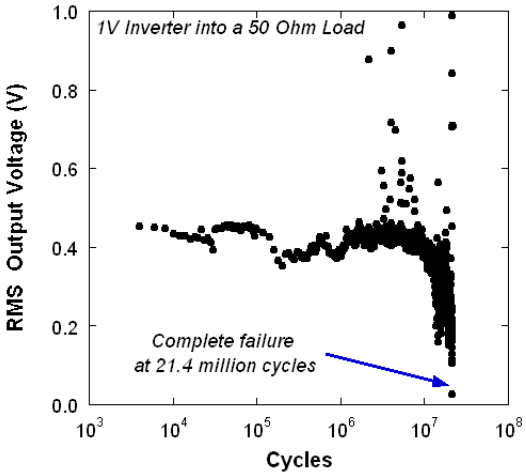

Figure 4: Inverter reliability with $5V_{DC}$ operation into a 50 Ohm load. Failure mode are currently under investigation with high contact resistance generated by contact contamination is a leading possibility.

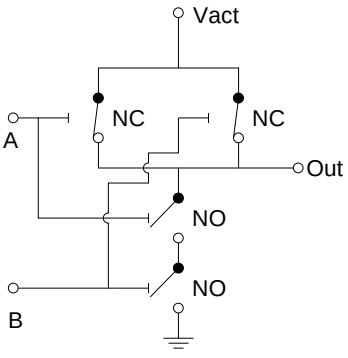

Figure 5: Schematic representation of a CML NAND gate based on using two normally closed (NC) switches in parallel, and two normally open (NO) switches in series.

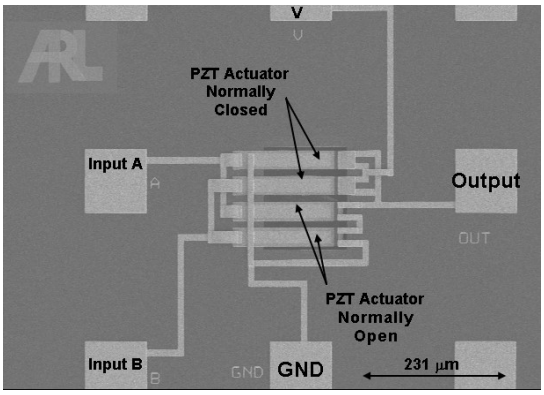

Figure 6: SEM image of a CML NAND gate with two normally closed and two normally open switches.

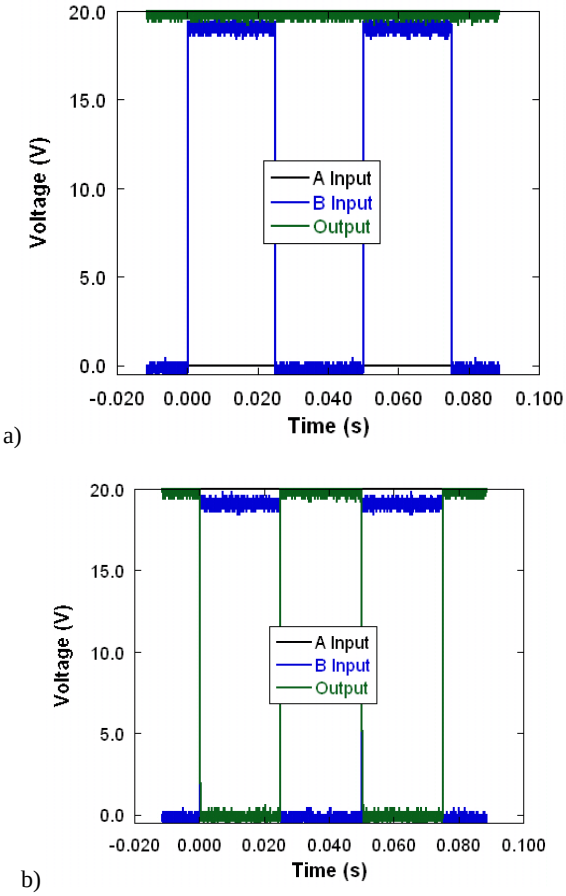

Figure 7: CML NAND gate experimental operation altering the A input between 0V (a) and 20 V (b).

In addition to the CML inverter, NAND gates and ring oscillators have been demonstrated. The NAND gate is shown schematically in Figure 6 and the actual device is shown in Figure 6. The typical CMOS inverter consists of two normally closed transistors wired in parallel to V_{act}, and two normally open transistors wired in series to ground (Figure 5). The CML NAND consists of two normally closed switches wired in parallel, and two

normally open switches wired in series, analogous to the CMOS implementation (see Figure 6).

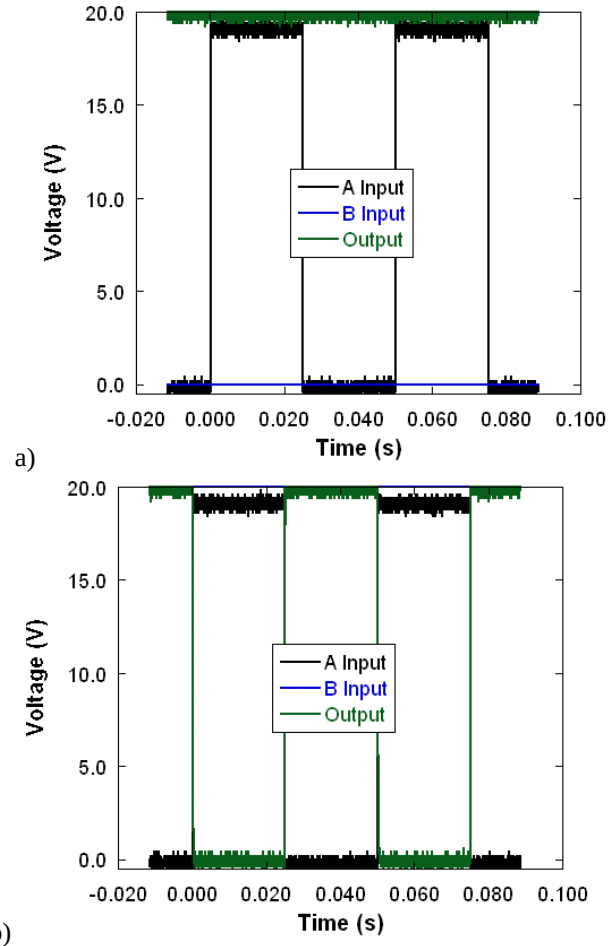

Figure 8: CML NAND gate experimental operation altering the B input between 0V (a) and 20 V (b)

The operation of the CML NAND gate is shown in Figure 7 and 8. A NAND gate has the interesting property that it behaves as a switchable inverter. For instance, when input A (black trace in Figure 7a) is high, then the signal on input B (blue trace in Figure 7a) is blocked, and the output is held high (green trace in Figure 7a). Conversely, if input A is held low then the input B signal is inverted on the output of the device (see Figure 7b). The opposite case, where input B is used to control the input A signal is illustrated in Figure 8. The successful NAND gates have only been operated at elevated voltages (at or near 20 V), although it is expected contact conditioning and actuator poling should allow for a decrease in operating voltage similar to the CML inverter.

Finally, a ring oscillator was successfully demonstrated using CML technology. A ring oscillator typically involves cascading an odd number of logic inverters and feeding the output of the last stage back to the first. This creates and instability which causes the output to toggle back and forth from high to low. Figure 9 shows the realization of the ring oscillator using MEMS logic. The SEM of the actual device is shown as the inset. A close inspection of the SEM shows the requisite odd number of inverters with the output section on the right feed back to the input section on the left. The output waveform is shown in the graph. The asymmetric waveform is believed to be due to different contact resistances for the normally open and normally closed switches. In addition we were only able to demonstrate the ring oscillator for a few seconds at a time. In most instances, the oscillations would stop after a few seconds of operation, but could be started again by turning the power on and off. We also believe the presumed contact asymmetry is responsible for the intermittent operation of this device. The long term stability and reliability of this device is currently being investigated.

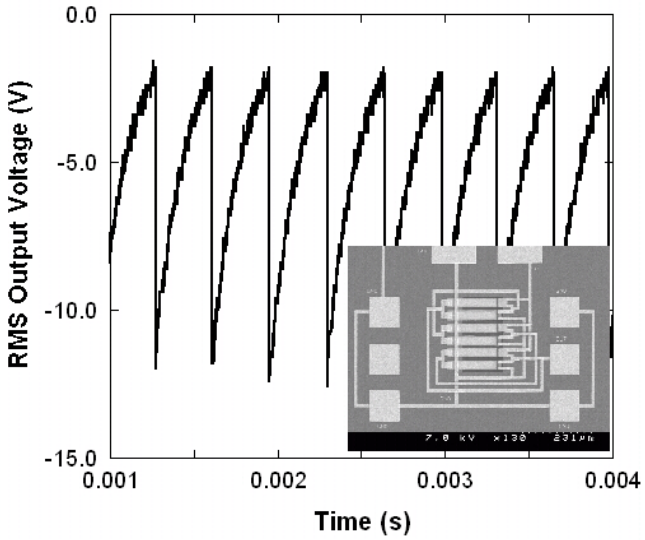

Figure 9: CML ring oscillator experimental performance with a frequency of operation of 2.9 kHz with an applied voltage of 11.2 V. The asymmetry in the output waveform is believed to be due to a difference in the NO and NC contact resistance. The actual device is shown in the inset SEM.

CONCLUSION

This effort has demonstrated low voltage CML components compatible with an existing PZT MEMS fabrication process. This could overcome the problems of integration of CMOS with our PZT process, and all of the potential process compatibility issues involved. One application that is currently being pursued is the integration of phase state control logic within the PZT phase shifter outlined in Reference 6. If successful, we could reduce the required 16 control inputs of a 4 bit phase shifter to 4 logic lines. The same technology can be applied to a wide variety of PZT MEMS components including PZT resonators [7] and microrobotics relying on PZT thin film actuators [8].

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