POROUS POLYSILICON SHELL FORMED BY ELECTROCHEMICAL ETCHING FOR ON-CHIP VACUUM ENCAPSULATION

Rihui He[1], Li Fan[2], Ming C. Wu[2], and Chang-Jin "CJ" Kim[1]
[1]Mecahnical and Aerospace Engineering Department,
[2]Electrical Engineering Department, University of California, Los Angeles (UCLA)
Los Angeles, CA 90095

ABSTRACT

We have developed a novel on-chip vacuum encapsulation technique, which turns a thick polysilicon layer porous "after deposition" so that the process is fully compatible with typical polysilicon surface micromachining. Once the polysilicon shell layer is deposited over the top sacrificial SiO_2 layer and turned porous, the thick porous layer allows for fast removal of sacrificial material underneath, but not the penetration of sealing materials during subsequent vacuum sealing. The sacrificial etching through a thick porous shell is confirmed visually, and the idea of sealing is proved with a dual cavity structure. To showcase the applicability, the proposed process is further demonstrated through the common MUMPs process.

INTRODUCTION

The on-chip packaging approach has long been recognized as a technology to simplify the subsequent packaging and thus reduce the cost of final MEMS product. This technology is especially beneficial to many resonating devices, which frequently require vacuum encapsulation. Despite the anticipated advantages over the usual post-process packaging methods that involve bonding, the monolithic on-chip encapsulation methods have some drawbacks and so far not proven practical.

In the early on-chip encapsulation techniques, the sacrificial layer was removed by allowing the etchant (e.g. HF) to enter the microshell through the lithographically-made etch holes on the shell [1, 2]. In addition to the long etching time and the resulting extended exposure to the etchant, which raises the concern for material degradation [3], the deposition of sealing material on the surface of the encapsulated devices is not negligible, affecting the device characteristics. The problem would be more serious for the recent devices with nanogap [4]. To overcome these drawbacks, thin (below 100 nm), permeable polysilicon, deposited by LPCVD in a certain process condition, was proposed as the shell material [5-7]. However, the permeability was in large part due to the thinness, requiring a separate thick shell layer and using the thin permeable polysilicon only at the etching holes on the shell. Further, a small amount (80Å) of sealing material still penetrated through the thin permeable layer during sealing.

The concept of the new on-chip encapsulation approach is shown in Fig. 1. What is desired is a thick but permeable shell layer, so that it can be a structural material by itself and also block the sealing material from passing through the pores during the vacuum sealing process. Among various porous materials, porous polysilicon is chosen because it can be turned porous by electrochemical etching "after" it is deposited, which makes the process compatible with typical polysilicon surface micromachining processes. If the thick polysilicon is made porous, with vertically-oriented nanopores preferentially, it satisfies most of the desired characteristics: structural layer by itself, resistant but permeable to HF, and effective sealing. The resulting on-chip encapsulation technology is expected to provide a low-cost, high performance packaging solution for a wide variety of polysilicon surface-micromachined devices, especially micro- and nano-resonators.

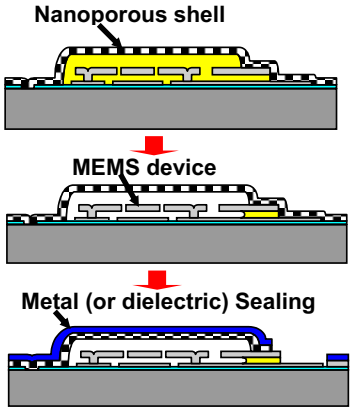


Figure 1. *On-chip encapsulation by thick porous shell*

FORMATION OF POROUS POLYSILICON SHELL

In the traditional electrochemical etching, porous polysilicon is directly formed on top of conductive material [8]. To be used for encapsulation in surface micromachining, the porous polysilicon needs to be formed on top of sacrificial layer, which is usually insulating oxide. Anderson *et al.* [9] has reported lateral porous etching of polysilicon formed between two nitride layers. However, the porous polysilicon layer was sacrificed to make nitride channel, rather than being released as freestanding structure. Since the voltage was applied between the channel ends, it is suspected that the pores are formed laterally and not suitable for our goal of passing the etchant through the thickness.

The process flow to test fabrication of freestanding porous polysilicon shell is outlined in Fig. 2. The 1.5 μm polysilicon shell was fabricated by typical polysilicon surface micromachining steps (Fig.2 (a)). The polysilicon was symmetrically doped from PSG layers on both sides by annealing at 1000 ºC in N_2. The polysilicon thus obtained a resistivity of 0.02 $\Omega \cdot cm$. In order to create an electrical

Travel support has been generously provided by the Transducers Research Foundation and by the DARPA MEMS and DARPA BioFlips programs.

contact between polysilicon and silicon substrate for electrochemical etching, openings were made through nitride layer to the silicon substrate.

After the top PSG layer was stripped off, the wafer was diced, and each die was mounted in the electrochemical etching set-up (Fig. 3). Photoresist was used as a simple mask to define electrochemical etching area. A photoresist with high resistance to electrochemical etching solution, NR 9-8000 negative photoresist, is used. Liquid In-Ga was painted on the backside of the sample to provide good electrical contact between the sample and the copper jig. The polysilicon was electrochemically etched in 49% HF:ethanol = 1:1 solution at 4 mA/cm^2 for 250 sec in room light and temperature. Then, the underlying PSG sacrificial layer was removed by HF, which diffuses through the pores of porous polysilicon. The HF release time was less than 2 minutes regardless of the size of the cavity. The sample was thoroughly rinsed in DI water and methanol. Final drying step used supercritical CO_2 drying to alleviate stiction problem (Fig. 2 (c)). Finally PECVD low stress nitride deposition was performed for vacuum sealing experiment (Fig. 2 (d)).

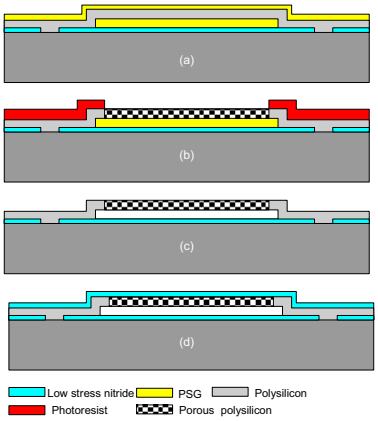


Figure 2. *Process flow of porous polysilicon shell formation, sacrificial etching, releasing, and sealing.*

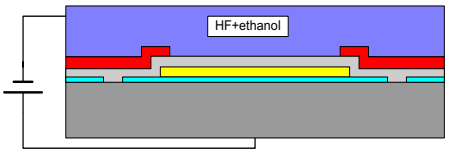
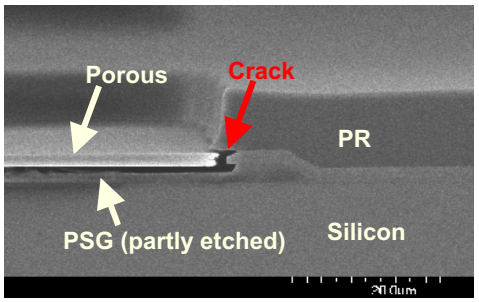
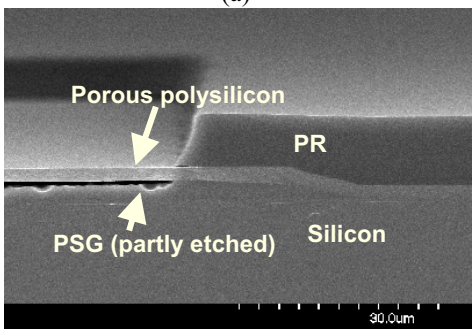


Figure 3. *Schematic view of the electrochemical etching set up. The backside is protected by a copper jig. Pt is used as the counter electrode in HF-ethanol solution.*

The electrochemical etching current has to be carefully chosen. In the electrochemical etching, pore growth rate increases with the current density [10]. In order to prevent photoresist from peeling off in the HF-ethanol electrochemical etching solution and to minimize etching undercut, high current density is preferred. However, high current density etching would create a problem of its own. Fig. 4(a) shows, after 140 sec electrochemical etching at 10 mA/cm^2, a crack is observed in the polysilicon under the edge of the photoresist mask. This is because after polysilicon in the unmasked area is turned porous, this small cross section area is exposed to etching solution and high current density leads to electropolishing of polysilicon. Fig. 4(b) shows the successful result of electrochemical etching when the current is lowered to 4 mA/cm^2. After 255 sec of etching, no electropolishing is observed in the polysilicon area protected by photoresist while the polysilicon in the unmasked area is already porous (indicated by the partial etching of PSG).



(a)



(b)

Figure 4. *SEM cross section images of the polysilicon shell after electrochemical etching at different current density. (a) 140 sec at 10 mA/cm^2, (b) 255 sec at 4 mA/cm^2.*

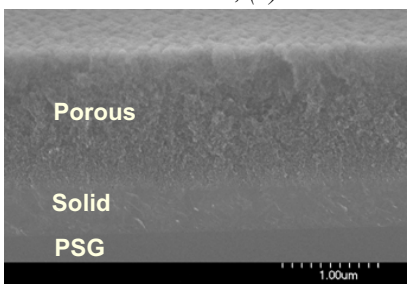


Figure 5. *SEM cross section of polysilicon shell after 200 sec electrochemical etching at 4 mA/cm^2 constant current*

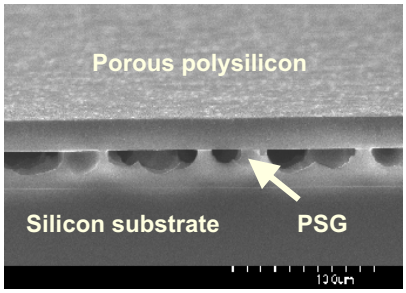


Figure 6. *SEM cross section of polysilicon shell after 250 sec electrochemical etching at 4 mA/cm^2 constant current.*

The process of pore growth during the electrochemical etching can be observed by SEM. Fig. 5 is a cross section of a sample after 200 sec of electrochemical etching. The polysilicon is turned porous in the top region, and the porous area is visually distinguishable from the solid area below. Fig. 6 is the SEM pictures of the cross section after 250 sec of electrochemical etching. There are many trenches observed at the top of PSG sacrificial layer, which indicates that the polysilicon shell has been completely turned porous and HF in the electrochemical solution has diffused through the porous polysilicon shell to attack PSG. The irregular etching pattern in PSG shows the pore growth across the shell area is not uniform. It is suggested that the electrochemical etching current flows mainly along the polysilicon grain boundaries, which leads to a higher pore growth rate and preferential etching of the grain boundaries [8].

Fig. 7 shows the interface of the porous and solid area near the edge of the porous polysilicon cavity. The left side of the shell is porous, while the right side is solid, which was protected by photoresist during the electrochemical etching.

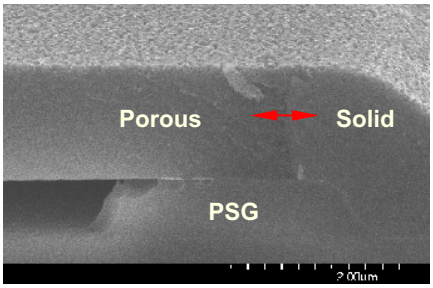


Figure 7. *SEM cross section of polysilicon shell. The interface of porous and solid area is visible. Photoresist, which protected the solid region during the porous etching, has been removed.*

VACUUM SEALING

We used a simple dual cavity design [5] to prove vacuum sealing on porous polysilicon shell. A 150 μm dual cavity with porous polysilicon shell was sealed by 1 μm PECVD low stress nitride deposition (Fig. 8). The deposition pressure was 900 mTorr. To ensure the air in the cavity is fully evacuated, the sample was pumped down in vacuum for more than 2 hours before the nitride sealing.

After the nitride deposition, the profile of one of the cavity was first measured by a Dektak profilometer. Then, the other cavity was broken intentionally by a probe tip before obtaining the profile of the first cavity again. The 1.63 μm height difference indicated the cavities had been sealed in low pressure during the PECVD nitride deposition.

The deflection of the cavity after vacuum sealing is calculated by the model in [11, 12]. The pressure load deflection relationship is given as:

$$p = \frac{C_1 \sigma t h}{a^2} + \frac{C_2 E t h^3}{a^4}, \quad Et = E_1 t_1 + E_2 t_2$$

The Young's modulus of porous polysilicon E_1 is roughly measured to be 30 GPa by load deflection experiment on a porous polysilicon membrane. The Young's Modulus of silicon nitride film E_2 is assumed to be 190 GPa from literature. Residual stress σ is deducted from the shell deflection when the pressure applied is 0. The calculated deflection h from this model is 1.68 μm, which is in good agreement with the measured deflection 1.75 μm.

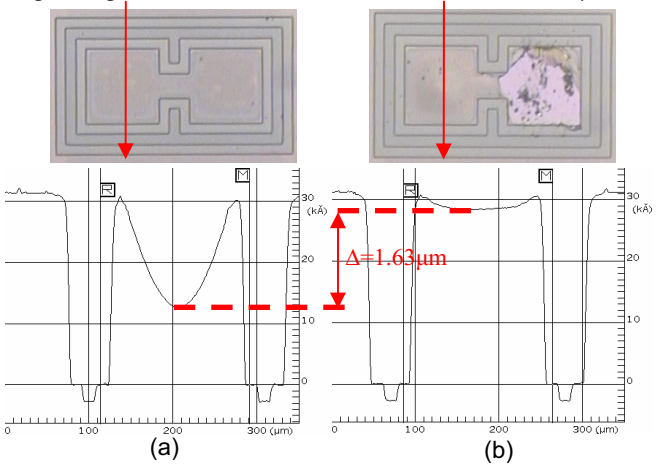


Figure 8. *A 150 μm dual cavity is used to prove sealing effect. Both of the scanning data are from the left cavity, indicated with the arrows. The scan data (a) was obtained before breaking the right cavity and the scan data (b) was obtained after the breakage.*

INTEGRATION WITH MUMPS PROCESS

To demonstrate the general application of this technique, Poly2 layer in MUMPs process has been chosen to form porous polysilicon shell. MUMPs service is widely used for polysilicon surface micromachining.

Fig. 9 is the schematic view of the process. A bridge resonator structure has been designed inside the shell to demonstrate on-chip encapsulation of microdevices. Poly2 layer on top will be partly turned porous by electrochemical etching. Supporting posts are designed to reinforce the polysilicon shell of the large size. The sacrificial oxide is used to isolate the polysilicon shell from the electrical feedthrough by time control of the release in HF.

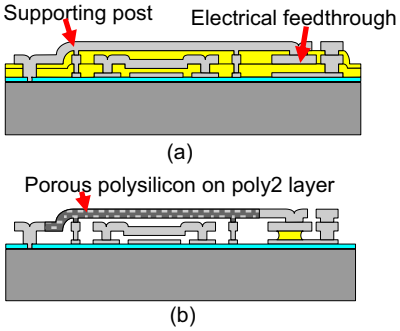


Figure 9. *Schematic view of a MUMPs device. (a) as received. (b) after post process to release bridge structures.*

The post process on the MUMPs chip starts with the removal of all the layers on the backside by RIE. This is necessary to open the electrical contact to the Poly2 layer through the substrate. Using photoresist as a mask, part of

the Poly2 shell is turned porous by electrochemical etching. The structure is then released in less than 4 minutes in 49% concentrated HF.

Fig. 10 is a microscopic top view of the device after release, which shows the color difference between the porous area and non-porous area on the polysilicon shell. Many black dots are observed on the porous polysilicon shell surface. Those black dots are identified as the area with higher porosity from the SEM observation.

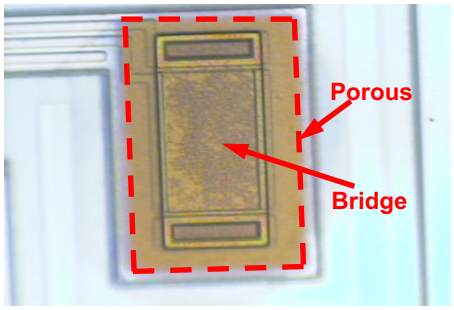


Figure 10. *Optical picture of a released bridge. The area inside the dashed line is the porous area on the Poly2 shell.*

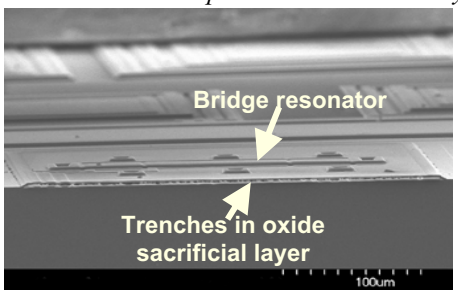


Figure 11. *SEM cross section of porous polysilicon shell on a MUMPs chip.*

Shown in Fig. 11 is the cross section of a device after electrochemical etching. The trenches in oxide indicate HF in the electrochemical etching solution has started to etch sacrificial oxide layer through the pores. The SEM picture in Fig.12 shows the bridge has been successfully released without any stiction.

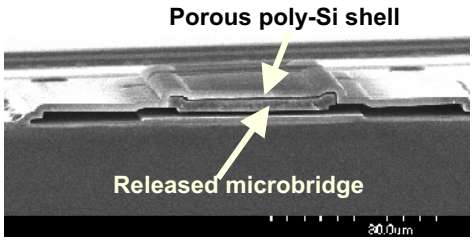


Figure 12. *A released microbridge on MUMPs chip.*

CONCLUSION

We have successfully demonstrated the first on-chip encapsulation using a porous polysilicon shell. The 1.5 μm polysilicon shell is completely turned porous in 255 sec by electrochemical etching. Porous area on the polysilicon shell can be simply defined by photoresist masking. The sacrificial layer under the porous polysilicon shell is cleared in 2 minutes (without device inside) or 4 minutes (with device inside) in 49% concentrated HF regardless of the shell area size. PECVD low stress nitride deposition has successfully sealed the cavity with porous polysilicon shell in vacuum. The process is fully compatible with typical surface micromachining process. Integrating with the common MUMPs process, a bridge structure is successfully encapsulated by this technique.

ACKNOWLEDGEMENT

This work was funded by DARPA MEMS Program. Discussion with Prof. B. Dunn is highly appreciated.

REFERENCES

[1] H. Guckel, D. W. Burns, C. R. Rutigliano, D. K. Showers, and J. Uglow, "Fine grained polysilicon and its application to planar pressure sensor," *Proceedings of the 4th International Conference on Solid-State Sensors and Actuators (Transducer '87)*, 1987, pp. 277-82.

[2] L. Lin, K. M. McNair, R. T. Howe, and A. P. Pisano, "Vacuum-encapsulated lateral microresonators," *Proceedings of the 7th International Conference on Solid-State Sensors and Actuators (Transducers'93)*, Yokohama, Japan, 1993, pp. 270-3.

[3] J. A. Walker, K. J. Gabriel, and M. Mehregany, "Mechanical integrity of polysilicon films exposed to hydrofluoric acid solutions," *Proceedings of the IEEE Micro Electro Mechanical Systems*, Napa Valley, California, USA, 1990, pp. 56-60.

[4] J. R. Clark, W.-T. Hsu, and C. T.-C. Nguyen, "High-Q VHF micromechanical contour-mode disk resonators," *Technical Digest of IEEE Int. Electron Devices Meeting*, San Francisco, California, 2000, pp. 399-402.

[5] K. S. Lebouitz, R. T. Howe, and A. P. Pisano, "Permeable polysilicon etch access windows for microshell fabrication," *Proceedings of the 8th International Conference on Solid-State Sensors and Actuator*, Stockholm, Sweden, 1995, pp. 224-227.

[6] K. S. Lebouitz, A. Mazaheri, R. T. Howe, and A. P. Pisano, "Vacuum encapsulation of resonant devices using permeable polysilicon," *IEEE MEMS Conference*, Orlando, FL, 1999, pp. 470-475.

[7] G. M. Dougherty, T. D. Sands, and A. P. Pisano, "Microfabrication using one-step LPCVD porous polysilicon films," *Journal of Microelectromechanical Systems*, vol. 12, 2003, pp. 418-24.

[8] P. G. Han, M. C. Poon, P. K. Ko, J. K. O. Sin, and H. Wong, "Study of luminescent porous polycrystalline silicon thin films," *J. Vac. Sci. Technol. B*, vol. 14, pp. 824-6, 1996.

[9] R. C. Anderson, R. S. Muller, and C. W. Tobias, "Porous polycrystalline silicon: a new material for MEMS," *Journal of Microelectromechanical Systems*, vol. 3, pp. 10-18, 1994.

[10] V. Lehmann, "The physics of macroporous silicon formation," *Thin Solid Films*, vol. 255, 1995, pp. 1-4.

[11] O. Tabata, K. Kawhata, S. Sugiyama, and I. Igarashi, "Mechanical Property Measurements of Thin Films Using Load-Deflection of Composite Rectangular Membranes," *Sensors and Actuators*, vol. 20, 1989, pp. 135-141.

[12] D. Maier-Schneider, J. Maibach, and E. Obermeier, "A new analytical solution for the load-deflection of square membranes," *Journal of Microelectromechanical Systems*, vol. 4, 1995, pp. 238-241.