HIGH-RESOLUTION ELECTROMETER WITH MICROMECHANICAL VARIABLE CAPACITOR

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ABSTRACT

We have designed, fabricated, and operated an electrometer with a noise-equivalent resolution of 535 electrons rms (86 aC). The electrometer incorporates a silicon resonator that acts as a variable capacitor and is fabricated using a new self-assembly process that demonstrates for the first time the integration of low-noise, low-leakage JFETs with SOI structures. The resolution of the measurements made with the electrometer thus far has been limited to 9500 electrons (1.5 fC) because of a large quiescent charge on the input, generated by JFET gate current. At 1.5 fC, the MEMS electrometer charge resolution is an order of magnitude better than those quoted for the best commercial instruments. Improvements that should lead to higher resolution are proposed.

INTRODUCTION AND THEORY

For over a century, scientists have used electrometers, instruments that measure electric charge, to study a variety of phenomena. Electrometers are used in mass spectrometers, scanning tunneling microscopes, and airborne-particle detectors, to name a few applications.

In 1947, researchers built an electrometer with a resolution of 4 fC (25,000 electrons). **[1]** Although recent research projects have demonstrated charge sensors with subelectron resolution using cryogenics **[2]** or magnetically levitated rotors **[3]**, there has been limited progress in developing practical electrometers for use in instrumentation. (The best commercial electrometer we are aware of is the Keithley 6514, which has a resolution of 10 fC) A fundamental difficulty in making a sensitive, low-frequency, solid-state electrometer is the high level of *1/f* noise associated with a dc measurement. In voltage amplifiers, *1/f* noise can be eliminated using the technique of chopper stabilization, typically implemented using MOS switches. MOS switching is not, however, well suited to electrometry because subthreshold leakage in the off-transistors and switch-charge injection impose a lower limit on the detectable charge value.

The instrument we describe uses the principle of input-capacitance modulation, which was also employed in the "vibrating-reed electrometer" of Palevsky et al. **[1]** To illustrate this technique, consider the basic electrometer circuit of Fig. 1. The charge to be measured, Q, is collected on a variable capacitor, C_V and a parasitic capacitor, C_P. The resulting dc voltage is

$$V = \frac{Q}{C_P + C_V}. \qquad [1]$$

If we let C_V vary sinusoidally, according to

$$C_V = C_0 + \hat{C}\cos\omega t, \qquad [2]$$

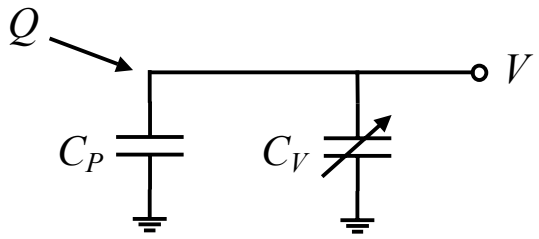

Fig. 1: *Basic input capacitance modulation circuit*

we expect to find a component of V at the modulation frequency ω. By performing a power-series analysis of Eqs. 1 and 2, we find the magnitude of this variation, normalized to the input charge:

$$\frac{\hat{V}}{Q} = \frac{\hat{C}}{(C_0 + C_P)^2}. \qquad [3]$$

Like the dc voltage, the modulated voltage is linearly proportional to input charge. However, the signal-to-noise ratio of the modulated voltage is typically orders-of-magnitude higher because of reduced *1/f* noise. Using synchronous detection at the modulation frequency, we can perform a charge measurement with a lower noise floor. If ω is sufficiently high, the effects of *1/f* noise are negligible.

Equation 3 implies that to obtain maximum signal the electrometer should have a large variable capacitance and small dc capacitances ($C_0 + C_p$). Large parasitic capacitances reduce the signal magnitude severely because of their contribution to the squared term in the denominator. Silicon micromachining allows one to fabricate air-gap variable capacitors with a high relative-capacitance change and a low parasitic capacitance, compared to macroscale devices. Thus, MEMS technology provides the means to build considerably improved electrometers that function according to well-established principles.

FABRICATION

The electrometer requires a technology that combines large capacitance variation, low parasitic capacitance, and low-noise, low-leakage transistors. A two-chip solution in which the variable capacitor and input transistor are located in separate packages performs poorly because of the large parasitic capacitances associated with the packages and interconnects. An integrated process combining CMOS and MEMS provides low parasitic capacitance, but this performance gain is cancelled out to some degree by the poor noise properties of the technology. CMOS transistors are characterized by relatively high *1/f* noise—electrometers invariably use a JFET input stage for this reason.

Our fabrication process includes a fluidic self-assembly step to conductively bond low-noise, low-leakage JFETs to high-aspect-ratio SOI structures. Since the backside of the JFET serves

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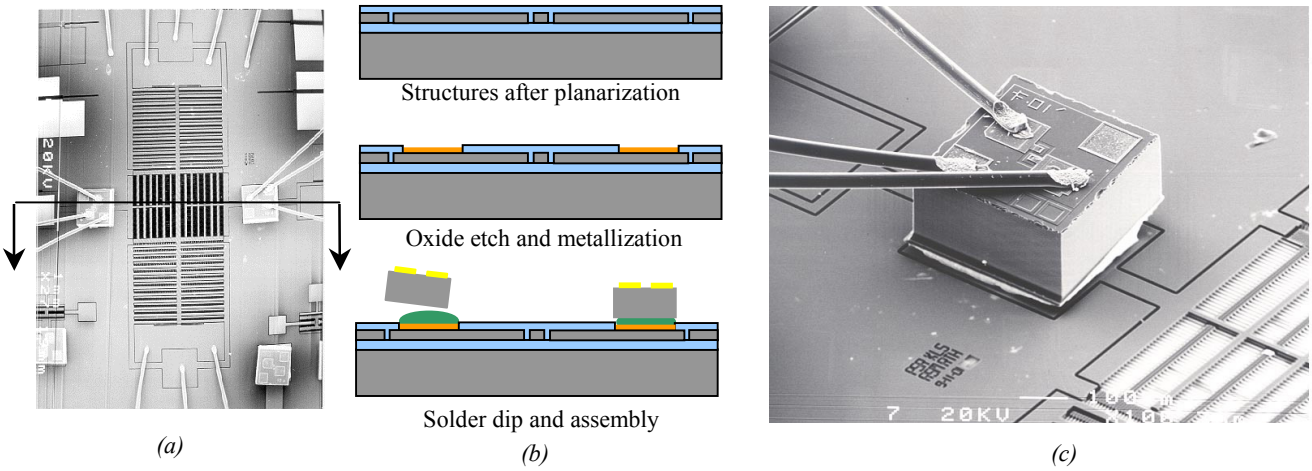

Fig. 2: *Illustrations of the electrometer chip. (a) Scanning electron micrograph of a functional electrometer with indicated line for process-flow cross section. (b) Process-flow cross sections. (c) Assembled and wirebonded JFET on SOI substrate. Wirebonding to the gate of the JFET is not necessary for the operation of the system, but a bond was made here for diagnostic purposes.*

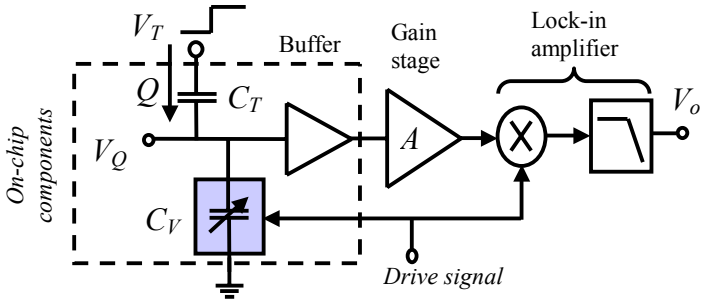

Fig. 3: *Electrometer block diagram.*

as a gate connection, it can be directly connected to a MEMS structure without introducing package parasitics.

The completed device with its corresponding cross section and process flow are shown in Figure 2. The starting SOI wafer has a 50-µm single-crystal silicon layer to be used for micromechanical structures, a 2-µm-thick sacrificial oxide layer, and a 500-µm handle layer. After patterning with 1-µm OCG 825 G-line photoresist, the structural layer was defined using a Surface Technology Systems (STS) deep reactive-ion etcher. **[4]**

Trenches were refilled and the wafer was planarized with PSG, deposited by LPCVD. The phosphorus was driven in and the film densified for 1 hour at 1050 °C. Lift-off, with 9-µm STR 1075 G-line photoresist, was used to define the JFET-gate electrical interconnects. The metallization used was Cr/Ni/Au (10nm/100nm/120nm) with the nickel layer acting as a diffusion barrier between the gold and silicon. The wafer was then covered with 2-µm G-line photoresist and diced. The gold pads were coated with a low-T solder (LMA-117, Small Parts Inc.), consisting of lead, tin, bismuth, cadmium, and indium by immersing the chips in the molten alloy at 70 °C through a DI water and acetic acid interface, pH 3. **[5]** The chips were soaked in concentrated HF for 7 minutes to release the structures. The dice were then rinsed with DI water to remove residual HF and placed into a 70 °C solution of DI water and acetic acid, pH 3, which inhibits oxide formation on the solder. A fluidic self-assembly process developed by Srinivasan **[6]** was used to align and bond the JFETs to the SOI structures. Assembly and self-alignment take place when the gold-plated underside of the JFET comes into contact with the molten alloy on the substrate site. After assembly, the dice were cooled to room temperature, rinsed with DI water, and dried using critical-point drying. Wirebonds were made to the source and drain of the JFETs, as well as to electrodes on the SOI structure. Measured resistances for the solder bonds are less than 5 Ω. The mechanical stability of the solder bonds is sufficient to withstand wirebonding using an ultrasonic wedge bonder (Westbond 7400).

ELECTROMECHANICAL DESIGN

Fig. 3 shows a block diagram of the electrometer system. In this prototype, charge is injected through a test capacitor C_T by applying a step voltage at V_T. The impedance of C_T was measured separately to calibrate the system. The charge accumulates on variable capacitor C_V, implemented by a micromechanical resonator. The resonator is driven by an external signal, which is also used as the reference frequency for the lock-in amplifier. A JFET source follower allows the voltage at V_Q to be buffered off-chip. Following the buffer, a low-noise instrumentation amplifier applies gain. A lock-in amplifier (Stanford Research Systems SRS850) performs the synchronous detection as well as storing and displaying the data. Only the input capacitor, the variable capacitor and the input transistor of the buffer are included on-chip in this implementation.

Resonator Design

The variable capacitor was implemented using an electrostatically driven lateral resonator in the SOI layer. The main drawback of this implementation is the possibility of coupling of the drive signal into the sense circuitry. Driving the structure in ambient air requires ac voltages of a few volts. Since the charges we wish to measure may only generate microvolts on the sense capacitor, it is necessary to take care to prevent any coupling from taking place. We use several methods to reduce this feedthrough, including shielding, differential drive and sense, and harmonic sensing.

Harmonic sensing refers to the technique of making the charge measurement at a harmonic of the drive frequency, rather than at the drive frequency itself. Since we need only sense in a narrow bandwidth around the sense frequency, the feedthrough at the drive frequency can be rejected by filtering. This technique has been used in an electrostatic voltmeter. **[7]** We devised a geometry of comb fingers that generates a sense voltage at twice

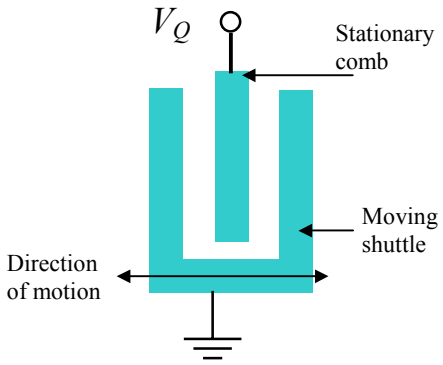

Fig. 4: *Balanced transverse comb*

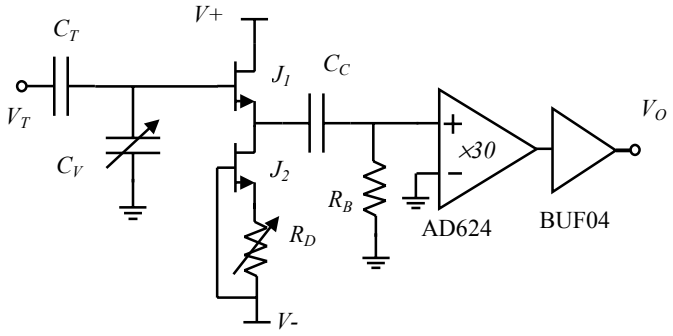

Fig. 5: *Electrometer circuit schematic*

the frequency of motion of the structure, the balanced transverse comb arrangement shown in Fig. 4. Due to the nonlinearity of the two opposing parallel-plate capacitors, each cycle of motion of the resonator generates two maxima and two minima of C_V. The resulting voltage at V_Q contains a component at twice the motional frequency when a charge is applied to C_V.

An overhead SEM of the resonator is shown in Fig. 2(a). We apply antisymmetric ac waveforms to the two opposing drive electrodes. Due to the symmetry of the structure, the effect of these two signals cancels out at the charge nodes.

Circuit design

Fig. 5 shows the circuit schematic for the electrometer. Table 1 gives the component values for the circuit. Although the system was designed with the option for differential circuits, the effectiveness of our other feedthrough-rejection mechanisms allowed us to use single-ended circuits for the measurements in the following section.

The source-follower circuit uses two JFETs (InterFet part#2N4117), an on-chip input device (*J1*) and an off-chip current source (*J2*). The output of the buffer is ac-coupled to the instrumentation amplifier to protect it from out-of-range voltages. The instrumentation amplifier is configured for a gain of 30. Its output is connected to an analog buffer to drive external loads. All of the components described are enclosed in a grounded metal box with BNC feedthroughs for critical signals.

EXPERIMENTAL RESULTS

The following methodology was used to make charge measurements using the prototype electrometer.

Using a dc potential of 15 V on both drive electrodes added to antisymmetric 5 Vp-p ac waveforms, we are able to drive the resonator with an amplitude of 2.7 µm, half of the gap spacing. The resonator has a measured resonant frequency of 2.6 kHz and a quality factor of 0.75. (Mechanical measurements were taken using the computer microvision system. **[8]**) Since the system is overdamped, it is advantageous to drive at a frequency below resonance. A drive frequency of 700 Hz was used.

Component	Value
C_T	156 fF
C_V	9 pF + 0.42 pF×cosωt
R_D	0-10 kΩ, 5 kΩ nom.
C_C	18 nF
R_B	22 kΩ
$V+/V-$	+6V/-6V

Table 1: *Electrometer circuit component values*

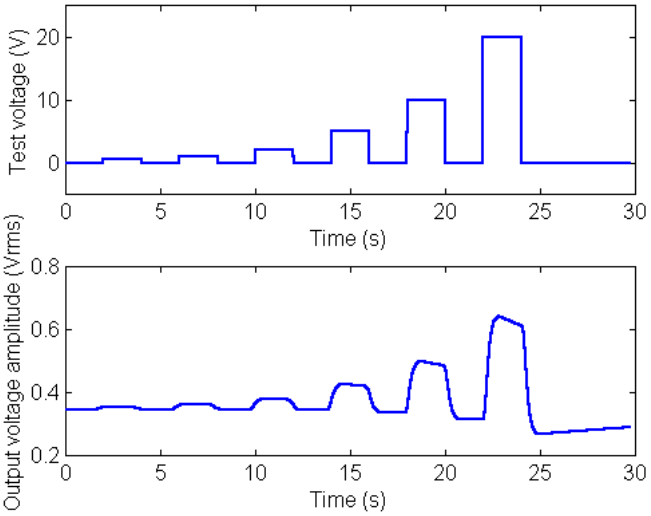

Figure 6: *Step-voltage series applied to test capacitor (top) with corresponding lock-in output trace (bottom).*

A known quantity of charge was injected onto the input by applying a step voltage on the input capacitor using a programmable voltage source (Keithley 2400 Sourcemeter). The output of the system was monitored using the lock-in amplifier. The signal at twice the drive frequency (1400 Hz) was selected. The raw data were analyzed in MATLAB to determine the step height ΔV_0 associated with each input charge ΔQ. An example data trace is shown in Fig. 6. After a positive V_T step, the input charge decays exponentially toward the equilibrium (starting) value with a time constant of roughly 15 s, hence the apparent shift in baseline signal when the opposite step voltage is applied.

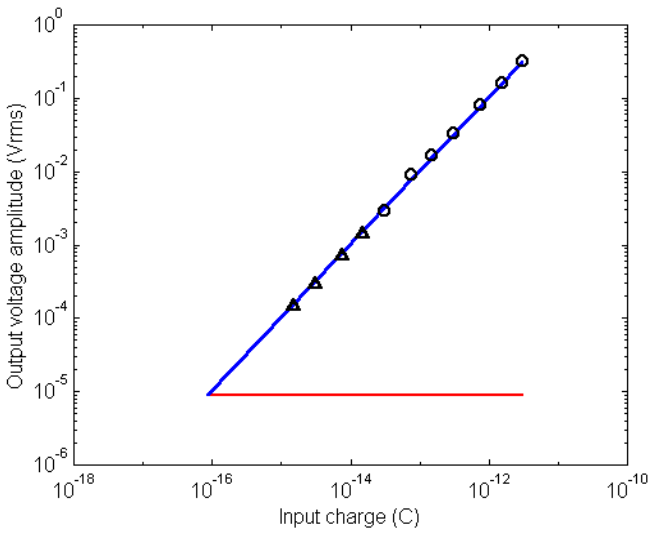

Figure 7: *Measured data from the electrometer with linear fit and noise floor in a 3.1 Hz bandwidth.*

A range of charge measurements is plotted in Fig. 7. The smallest charge measured was 1.5 fC (9500 electrons) and the largest was 3 pC (19,000,000 electrons). The circles and triangles represent measurements taken using different lock-in-amplifier settings. The series represented by circles used a lock-in bandwidth of 1 Hz and a full-scale voltage of 1V. The series represented by triangles used a 3.1 Hz bandwidth and 50 mV full-scale. The maximum relative error of the entire series with respect to a linear fit is less than 15%.

Also plotted on Fig. 7 is the noise floor of the lower-range measurement, which was determined using a dynamic signal analyzer, and confirmed by observing the lock-in amplifier trace with no drive voltage applied. The input-equivalent voltage-noise density is 166 nV/√Hz. This corresponds to an input-equivalent charge of 86 aC (535 electrons) in the 3.1 Hz lock-in bandwidth.

The dominant limitation on the present system is that, in equilibrium, a quiescent charge of 4.5 pC is present on the input node. This charge is the result of the gate-leakage current of the JFET, which balances the leakage current to ground at an input voltage of 0.5 V. The presence of this charge generates a quiescent signal of 0.35 mVrms at the system output. This signal limits the gain we are able to use in the instrumentation amplifier and the lock-in amplifier. As a result, because the data-acquisition system has a limited dynamic range, we are not able to measure charges on the order of the noise floor. Data series 2 (triangles) was taken by initially applying a large negative pulse to V_T to clear the quiescent charge. We were then able to make small-charge measurements using a high-gain setting before the input charge returned to equilibrium. The leakage rate prevented the accurate measurement of any smaller charges.

In addition to the dc component of charge leakage, there is a random component. The rms random leakage current in a 1-minute measurement was 20 fA. The majority of this noise is at frequencies lower than 1 Hz.

The feedthrough signal at the sense frequency is less than 13 μV at the output. This signal is equivalent to a constant 120 aC (752 electrons) at the input. We measured this voltage when applying zero dc bias to the resonator, so that in theory no motion would occur. It is not clear whether the observed signal is, in fact, due to feedthrough, or due to motion of the structure because of a slight force imbalance between the opposing drive combs. In either case, feedthrough is not a limiting factor on sensitivity in the present measurement range.

CONCLUSIONS

The electrometer reported here has a higher measured resolution than that of the best available commercial instrument. Moreover, our noise analysis indicates that the measured performance can be improved. The present system should be capable of resolving 20 electrons in a 1 Hz bandwidth if only electronic thermal noise sources were present. In order to achieve this performance, we will have to identify and eliminate extraneous noise sources and solve the leakage problem. We believe that the quiescent charge can be cancelled using another JFET connected so as to apply an equal and opposite leakage current. Differential operation should also help with the quiescent-charge problem, as well as reject any common-mode feedthrough signals. We have in hand an electrometer fabricated in an integrated CMOS/MEMS process that addresses these issues. Tests are underway to determine the sensitivity of this system.

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