A LOW TEMPERATURE BI-CMOS COMPATIBLE PROCESS FOR MEMS RF RESONATORS AND FILTERS

Jennifer L. Lund, Christopher V. Jahnes, Hariklia Deligianni, L. Paivikki Buchwalter, John M. Cotte, Panayotis Andricacos, David E. Seeger, and John H. Magerlein
IBM T. J. Watson Research Center
Yorktown Heights, NY 10598

ABSTRACT

A low temperature, Bi-CMOS compatible process for the fabrication of MEMS resonators and filters has been developed. These devices hold the promise of reducing cost and power requirements in IC's for communications applications. The devices were fabricated on 200mm wafers in standard production tools using materials and processes routinely employed for on-chip interconnect in a typical CMOS line. The maximum processing temperature for the MEMS devices is 400C.

Simple cantilever and fixed beam structures were fabricated and tested. Un-encapsulated devices were measured in a low-pressure system to determine frequency response and quality factor (Q). Devices were typically actuated with DC biases between 4-5 V; useful tuning range is from ~3-7 V, corresponding to a 1% shift in frequency for the devices measured here. Frequency responses from 3-45 MHz have been recorded. Under vacuum, average device Q's were around 2000, although values above 10,000 have been measured. The devices maintain peak Q up to a pressure of approximately 100 mT. Temperature effects were also studied.

INTRODUCTION

The potential for MEMS devices to have a great impact on the communications industry has been widely discussed recently [**1**]. MEMS RF switches, reference oscillators, filters, and varactors are a few of the devices that could replace expensive and bulky off-chip passive components. It has even been proposed that MEMS filters could dramatically alter today's typical RF front-end architecture [**2**].

For resonators and filters aimed at replacing passive components in RF communications circuitry, the most critical design factors are ability to reach the frequencies of interest (~900MHz-2.1GHz), low power and/or bias voltages, size, and cost. To meet these needs, high-modulus/low-density materials must be used, aggressive scaling of both beam and gap dimensions is required, and straightforward integration with analog IC processes is desirable. A wide variety of materials have been used to form MEMS resonators, including polysilicon [**3,4**], single crystal silicon [**5,6**], SiO_2 [**7**], Si_3N_4 [**8**], Ni, poly-SiGe [**9**], and a variety of piezoelectric films. Similarly, there are a number of means of exciting and detecting resonance; electrostatic actuation is most common but magnetic [**8**], thermal [**7**], and optical [**10**] methods have been used. Finally, the varied geometries of MEMS resonators include comb-drives, which typically resonate in the kHz range, diaphragms, simple bridge and cantilever beams, torsional elements, and circular disks, which have been reported at frequencies as high as 156 MHz [**11**].

The MEMS resonators and filters demonstrated here are simple cantilever and fixed beam structures that use electrostatic actuation. Our preliminary design goals included low actuation voltages (< 6V), intermediate frequencies (~few 100 MHz), and the use of fabrication techniques that would allow the devices to be seamlessly integrated with the interconnect levels of high-speed CMOS or Bi-CMOS processes. The latter constraint leads to a maximum processing temperature of 400C and a somewhat limited set of materials. The resulting process was developed and run at the IBM Semiconductor Research and Development Center, where IBM's SiGe Bi-CMOS processes are qualified.

PROCESS DEVELOPMENT

Device fabrication begins with the lower metal level, which forms the drive and sense electrodes for the resonator, as well as the physical anchor points for and electrical contact to the beam. This metal level may be shared with other interconnect levels, such as a copper wiring level or a local interconnect level using a refractory metal (e.g., tungsten). The next step is the formation of a cavity for device encapsulation. The cavity serves two functions: to physically protect the device, and to assist in providing a low-pressure ambient for device operation. It has been repeatedly demonstrated that pressure is the greatest limiting factor on the achievable quality factor (Q) for MEMS resonators. This cavity may be comprised of one or more of the inter-layer dielectric (ILD) films used in the chip interconnect levels. Next, the sacrificial layer that forms the gap between resonator and electrode is deposited. Gaps between 300-3000Å were fabricated; nominal thickness of 1000Å was used in the process. The sacrificial material is patterned to allow contact between beam and lower metal (beam anchors). Then the beam materials, which consist of a thin metal layer followed by a thick dielectric layer, are deposited and patterned. Beam thicknesses from 0.6–1.0µm were used in this process, although thicker beams may be made. Fig. 1 shows a schematic of these process steps; Fig. 2 and Fig. 3 show SEM cross-sections of a cantilever beam resonator at this stage.

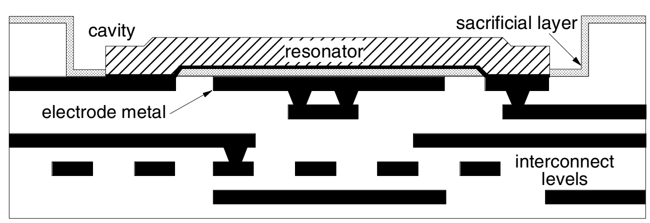

Fig. 1. *Initial process steps include formation of lower metal electrode layer and cavity for device encapsulation, followed by deposition and patterning of sacrificial layer and beam materials.*

The cavity is then refilled with additional sacrificial material, planarized, and sealed with a dielectric membrane, as shown in Fig. 4 and Fig. 5. The target thickness of the "upper" gap was 2500Å; however, planarity of the sacrificial material within the cavity was challenging to control and depended on the sizes of both the beam and the cavity. To solve this problem in subsequent runs, we reversed the order of formation of the beam and "cavity". This change allows us to planarize the additional ILD material

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rather than the sacrificial material (a process which is well known and practiced), and has the additional advantage of making the formation of thicker beams easier.

The sacrificial material must now be removed from the bulk of the cavity and from beneath the beam. Small vias are etched through the top membrane, and the sacrificial material is removed with a dry release process. Using this process, we have been able to easily undercut beams with gap thicknesses of as little as 300A (Fig. 6, left), and also to evacuate very large, deep cavities. Fig. 8 shows a FIB cross-section of a resonator beam after this procedure.

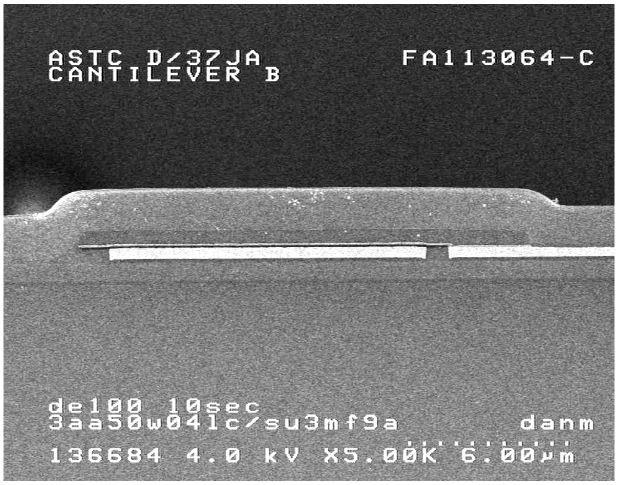

Fig. 2. *SEM cross-section of an un-encapsulated cantilever beam resonator prior to release (the material coating the beam is quartz deposited during SEM sample preparation).*

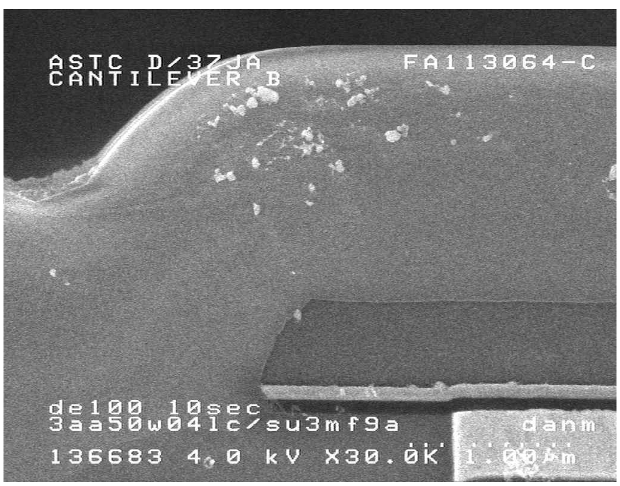

Fig. 3. *Expanded view of the tip of the cantilever beam of Fig. 2, more clearly showing the metal and dielectric layers of the beam, the gap, and the lower electrode. The total beam thickness is approximately 6500Å; the gap spacing is 1000Å.*

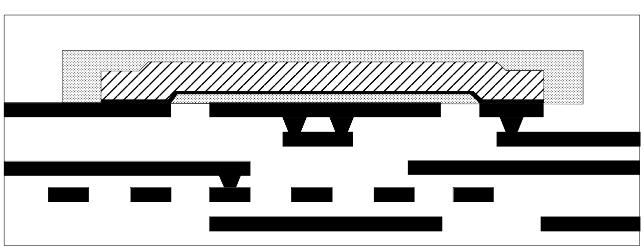

Fig. 4. *The device is surrounded with additional sacrificial material, and sealed inside a planarized cavity.*

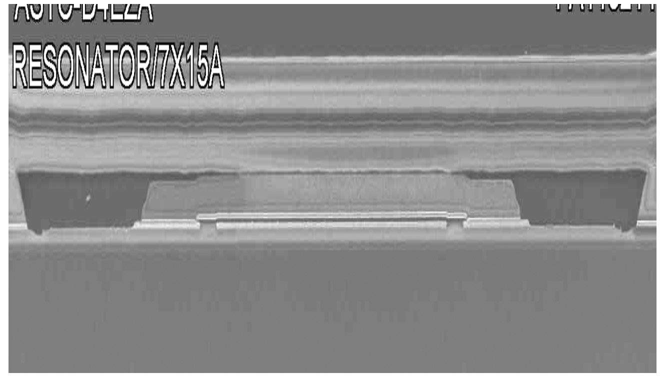

Fig. 5. *SEM cross-section of an encapsulated fixed beam resonator prior to release. The photo has been expanded in the z-direction to emphasize the gaps above and below the beam.*

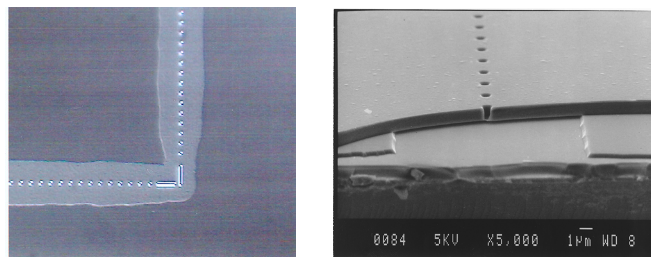

Fig. 6. *Demonstration of release of sacrificial layer through vias for a 300Å thick film (left, optical top-down photo) and a 2700Å thick film (right, SEM cross-section).*

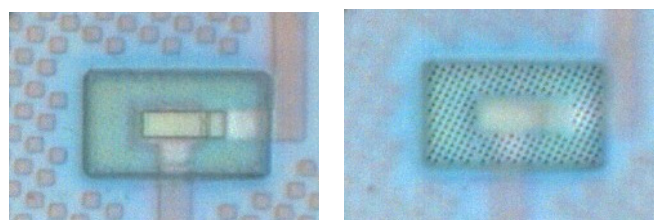

Fig. 7. *Optical photograph of a cantilever beam resonator after release through vias. On the left, focus is on the beam; on the right, focus is on the vias holes in the cavity membrane.*

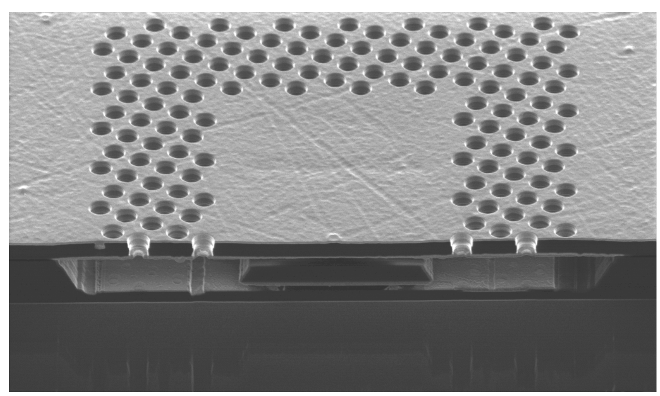

Fig. 8. *FIB cross-section showing evacuated cavity and freestanding fixed beam resonator after release through vias.*

Following release, the vias are re-sealed with an additional plasma-enhanced chemical vapor deposited (PECVD) film (Fig. 9 and Fig. 10). These two steps (release and sealing) can be done in a single tool, allowing a low pressure ambient within the device cavity. The “pinch-off” process can also be started in a PECVD tool and finished in a UHV tool such as a sputtering system if lower initial cavity pressures are desired. For limiting re-deposition inside the cavity during the pinch-off process, the size of the release vias is relatively unimportant as long as the aspect ratio remains above 4 (see Fig. 11). We selected 0.25µm vias with a depth of 1.0µm. To further limit effects of re-deposition on beam mass, release vias are not placed within 1.0µm of the device.

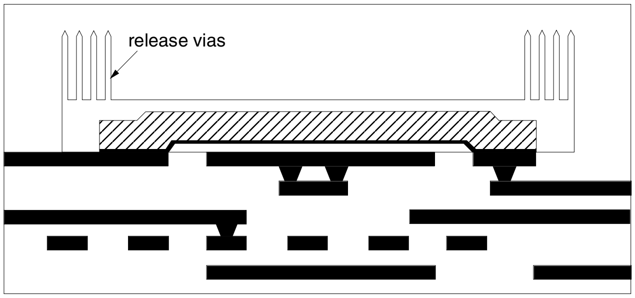

Fig. 9. *Release vias are etched in the cavity ceiling, and the sacrificial material is removed through the vias using a dry process. The vias are then sealed with an additional dielectric deposition.*

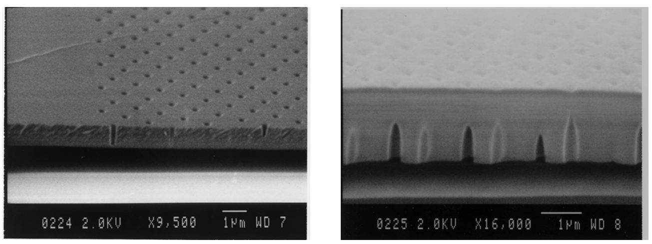

Fig. 10. *SEM cross-sections showing removal of a 1µm thick sacrificial layer through vias, and pinch-off of those vias with a second dielectric deposition. Note the cleanliness of the cavity floor beneath the vias.*

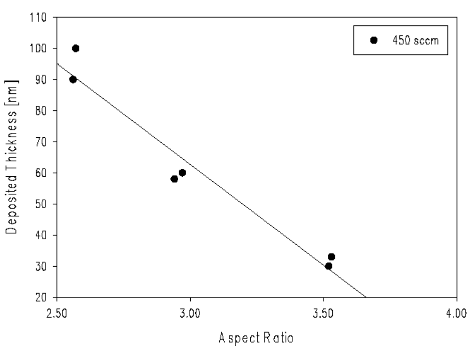

Fig. 11. *To limit re-deposition inside the cavity, release via aspect ratios should be kept above 4.*

RESULTS

Two basic beam sizes and configurations were characterized for frequency response and Q: 4µm x 10µm and 7µm x 15µm fixed beams and cantilever beams. Smaller beams were also fabricated but have not been successfully measured. Un-encapsulated devices were characterized so that the measurement pressure could be known and controlled. Except where specifically noted otherwise, the measurements reported here are for typical pressures of 30-50 µTorr and at room temperature. Measurements were taken on-wafer using microwave probes and an HP8753B network analyzer. Generally, DC bias and input power were applied to the beam, and transmitted power was measured from the grounded lower electrode. The plots below give S_{21} log magnitude vs. frequency; typical input power is –20 dBm and bias voltages are noted.

Fig. 12 and Fig. 13 show typical frequency responses for the fixed beam and cantilever beam resonators. While we have only been able to detect the fundamental mode for the fixed beam resonators, the cantilever beams reliably exhibit frequency responses corresponding to two different modes. Simple theory can predict these frequencies. Using:

$$f_i = \frac{\xi_i^2}{4\pi\sqrt{3}} \sqrt{\frac{E}{\rho}} \frac{t}{l^2}$$

where ξ_1 = 1.875, ξ_2 = 4.694 for the cantilever beam and ξ_1 = 4.730 for the fixed beam [12], and assuming t = 0.65µm, ρ = 3.1 gm/cm^3, and E = 160 GPa, this yields:

		Predicted [MHz]		Measured [MHz]	
		1st mode	2nd mode	1st mode	2nd mode
Cantilever Beam	15µm	3.35	21.01	3.05	21.35
	10µm	7.54	47.27	7.32	45.15
Fixed Beam	15µm	21.33	-	21.83	-
	10µm	48.00	-	42.32	-

Table 1. *Predicted and measured values of f_0 for fixed and cantilever beams.*

Note that the values of E and ρ used in the calculation are fitted parameters; 3.1 gm/cm^3 is a typical value for ρ and nanoindentation measurements of the dielectric layer of the beam gave values of ~190 GPa for E. A more accurate means of determining the material properties of the composite beams will be desirable.

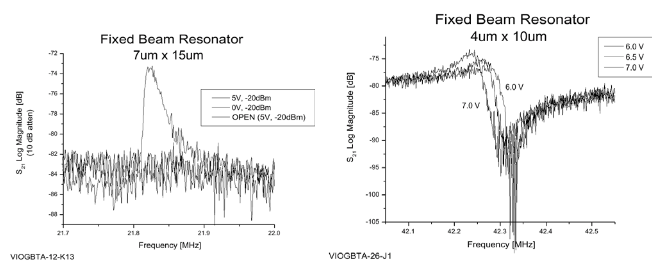

Fig. 12. *Frequency response of fixed beam resonators. For the 15µm beam (left), measurements at 0V DC bias and an open circuit are shown for reference. For the 10µm beam (right), voltage tuning is demonstrated.*

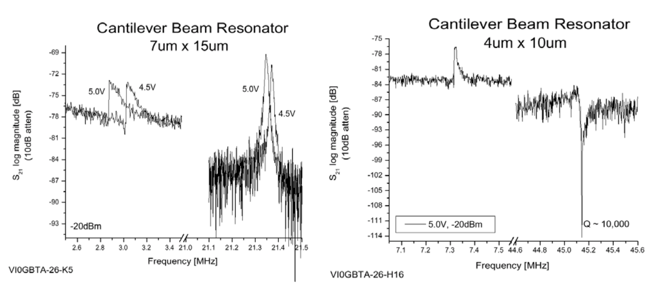

Fig. 13. *Frequency responses of cantilever beam resonators. Cantilevers reliably show responses that correspond to more than one mode. Voltage tuning is also shown for the device on the left.*

Figs. 13, 14, and 15 also demonstrate an important property of MEMS resonators: voltage tuning. In order to achieve target frequency and stability specifications for resonators in communications circuits, extraordinary process control will be required, particularly as the beams are scaled to smaller dimensions. Given process and, more importantly, material property variability, it is unlikely that these specs can be met without some method of actively tuning the resonant frequency. Although not yet completely characterized, we see here (Fig. 14) a 1% change in frequency over the range of 3.2-5.0V DC bias.

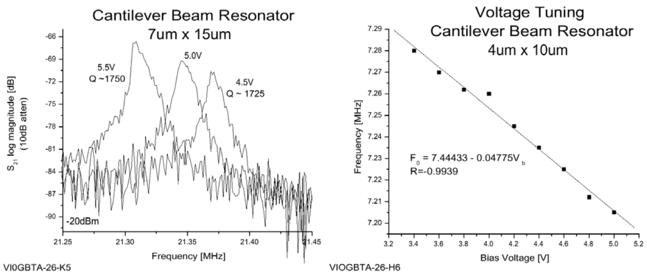

***Fig. 14.** Effect of bias voltage on center frequency and Q for a cantilever beam resonator.*

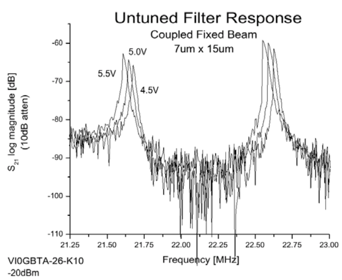

***Fig. 15.** Two peaks are exhibited by a coupled fixed beam filter structure. The bias voltages were not tuned independently in this measurement.*

The effects of pressure and temperature on resonant frequency are displayed in Fig. 16 and Fig. 17. As expected, Q decreases with increasing pressure, although peak Q is maintained up to about 100 mT. It is possible that the on-chip encapsulation method may not be able to maintain a long-term partial pressure in the mT range. Temperature variation from 25C to 85C yielded less that 0.15% change in center frequency for the fixed and cantilever beams in Fig. 17. This is well within the 1% tuning range noted above, and indeed is somewhat less than the device-to-device and day-to-day measurement variability that was typically found.

Finally, reliability data is anecdotal at this point. Several devices have been left operating overnight with no ill effects; the longest has been left for 18.5 hours at 22 MHz (over 10^{12} cycles).

CONCLUSIONS

MEMS resonators have been fabricated using processes and materials that are commonly found in the interconnect levels of CMOS and BiCMOS IC's. The maximum processing temperature for these devices is 400C, making it possible for them to be integrated directly on-chip without affecting the existing analog circuitry. These devices operate in the intermediate frequency range and exhibit the very high Q-factors characteristic of mechanical resonators. The ability to excite higher-order modes has been demonstrated. Voltage tuning, which can compensate for process and temperature variations, has also been shown.

The long-term efficacy of the wafer-level encapsulation process described here has not yet been assessed. Even if it should prove to be insufficient for maintaining a low pressure ambient without additional packaging solutions, wafer-level encapsulation is still critical for physical protection of the devices.

Scaling of MEMS resonators to achieve higher frequencies remains a distinct challenge. Very low signal-to-noise ratios will make driving and sensing these beams difficult. Furthermore, the very high impedance and effective Q of very small beams make their practical utility in analog circuit design an open question.

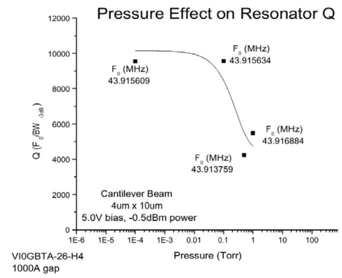

***Fig. 16.** Resonator damping increases with increasing pressure, although peak Q is maintained up to about 100mT.*

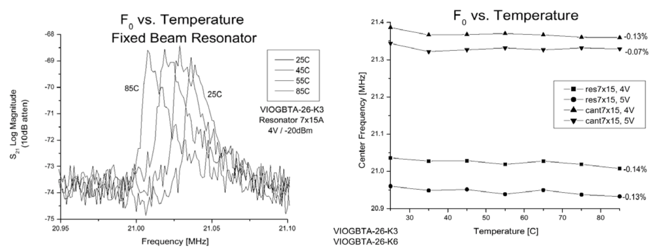

***Fig. 17.** Effect of temperature on frequency response for fixed beam and cantilever beam resonators.*

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REFERENCES

1. P. Gelsinger, remarks at Intel Developer Forum, 28 Feb. 2002.
2. C. Nguyen, A.-C. Wong, and H. Ding, "Tunable, switchable, high-Q VHF MEMS bandpass filters," *Dig. ISSCC*, (1999) pp. 78-79.
3. F. Bannon, J. Clark, and C. Nguyen, "High frequency micro-electromechanical IF filters," *Proc. IEDM*, (1996) pp. 773-776.
4. K. Wang, A.-C. Wong, and C. Nguyen, "VHF free-free beam high-Q microelectromechanical resonators," *MEMS '99*, (1999) pp. 453-458.
5. R.A. Buser and N.F. de Rooij, "Capacitively activated torsional high-Q resonator," *Proc. MEMS '90*, (1990) pp. 132-135.
6. J. Weigold, *et al.*, "A merged process for thick single-crystal Si resonators and BiCMOS circuitry," *J. MEMS, 8*, 3 (1999), pp. 221-228.
7. O. Brand *et al.*, "Thermally excited silicon oxide beam and bridge resonators in CMOS technology," *IEEE Trans. on Electron Devices, 40*, 10 (1993), pp. 1745-1753.
8. D. Greywall, "Micromechanical RF filters excited by the Lorentz force," *J. MEMS, 9*, 1 (1999), pp. 78-84.
9. A. Franke, *et al.*, "Post-CMOS modular integration of poly-SiGe microstructures using poly-Ge sacrificial layers," *Tech. Dig. 2000 Solid State Sensor and Actuator Workshop*, (2000), pp. 18-21.
10. T. Lammerink, M. Elwenspoek, and J. Fluitman, "Optical excitation of micro-mechanical resonators," *Proc. MEMS '91*, (1991), pp. 160-165.
11. J. Clark, W.-T. Hsu, and C. Nguyen, "High-Q VHF micromechanical contour-mode disk resonators," *Proc. IEDM*, (Dec. 2000), pp. 493-496.
12. W. Weaver, S. Timoshenko, and D. Young, *Vibration Problems in Engineering*, John Wiley & Sons, New York, 1990.