A High-Performance Hybrid CMOS Microaccelerometer

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ABSTRACT

A hybrid microaccelerometer subsystem consisting of an all-silicon μg capacitive microaccelerometer and a CMOS capacitive interface circuit is presented. The measured sensitivity for a device with 2mm x 1mm proof mass and 1.4μm air gap is 1.4pF/g and the calculated mechanical noise floor for the device is 0.39μg/√Hz in atmosphere. The circuit has a 95dB dynamic range, a low offset of 370μV and can resolve better than 75aF. The complete module has a measured sensitivity of 160mV/g and noise floor of 3.6μV/√Hz (-110dBV/√Hz), indicating that the current system is capable of resolving about 20μg/√Hz.

Keywords: Inertial sensors, μg accelerometer, interface circuit.

INTRODUCTION

High-precision microaccelerometer subsystems are needed in navigation/guidance, microgravity measurements, tilt control, platform stabilization, and position sensing [**1,2**]. The sensor should have high sensitivity, low temperature sensitivity, and good long-term stability. The interface circuit should have good dc response, low offset, and high offset and gain stability. Surface micromachined accelerometers attain high capacitive readout sensitivity by integrating the sensor and its interface circuitry [**2**]. However, these sensors typically have a noise floor of several 100μg's because of their small proof mass and small full-scale capacitance change. Bulk micromachined accelerometers have higher sensitivity and hence can attain sub-10μg/√Hz performance [**3**]. In this paper, we report the implementation and testing of a hybrid capacitive silicon microaccelerometer subsystem with a CMOS readout interface for high-precision applications mentioned above.

μg ACCELEROMETER STRUCTURE

A precision μg microaccelerometer is typically operated in closed-loop to obtain higher bandwidth, full-scale range, and linearity. For a high performance accelerometer, the main design consideration for the device structure is meeting the resolution specification which is determined by its mechanical and readout electronics noise. Mechanical noise can be reduced by increasing the size of the proofmass and reducing damping. Electrical signal-noise ratio can be improved by reducing electronic noise, and increasing proofmass size and device capacitance variation. The latter two provide a larger signal pick-up and result in less stringent readout circuit requirements. Mechanical noise is mainly due to Brownian motion and can be expressed in terms of mass size and total damping [**4**]. The key element in obtaining low mechanical noise floor without vacuum packaging is increasing mass size and controlling damping [**3,4**].

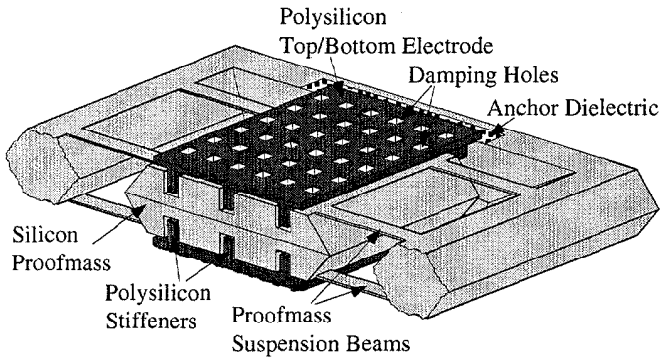

Figure 1. *Microaccelerometer structure [3].*

Our approach, as shown in Figure 1, addresses all these design issues by combining surface and bulk micromachining in order to achieve high device sensitivity, low noise floor, and controllable damping - all by using a single silicon wafer [**3**]. The central idea behind the process is to use the whole wafer thickness to attain a large proofmass, to utilize a sacrificial thin film to form a uniform and conformal gap over a large area, and to create electrodes by depositing polysilicon on the wafer. These electrodes, while thin, are made very stiff by embedding thick vertical stiffeners in them so that force rebalancing of the proofmass becomes possible [**5**]. The technology utilizes a trench refill technique to form thick stiffeners by depositing thin polysilicon films. Any damping hole configuration and geometry can be easily formed on the poly electrodes to optimize damping coefficient and capacitance, while there is no concern with large hole density and its effect on the electrode softening as the plate stiffness is mainly provided by the embedded stiffeners. There are eight boron-doped suspension beams which are symmetric with respect to the proofmass centerline and result in low cross-axis sensitivity. The electrodes are polysilicon plates created on both sides of the proofmass and anchored on an isolation dielectric at the frame.

FABRICATION PROCESS / RESULTS

The fabrication process, as shown in Figure 2, requires six masks and provides a yield of >80%. The process starts with a shallow (3μm) p++ boron diffusion on <100> double-polished p-type Si wafers. Both sides of the wafer are patterned and the patterns are aligned to each other. The shallow boron diffusion is performed at 1175°C for 30min and defines the beams, the

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proofmass and the supporting rim. Then, 5000Å of LPCVD oxide is deposited and patterned to form dimples. These dimples reduce the contact area and help reduce stiction. They also limit the range of travel and help against shock. The oxide also serves as a mask for the trench etch step. Next 40-60μm deep, 6μm wide trenches are etched in the silicon to be used later to form the vertical electrode stiffeners.

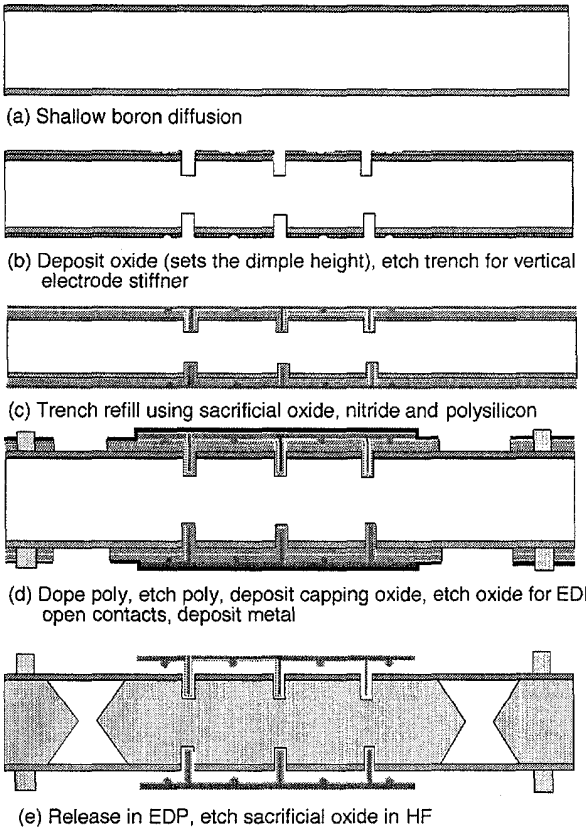

Figure 2. *Fabrication process sequence of a μg accelerometer.*

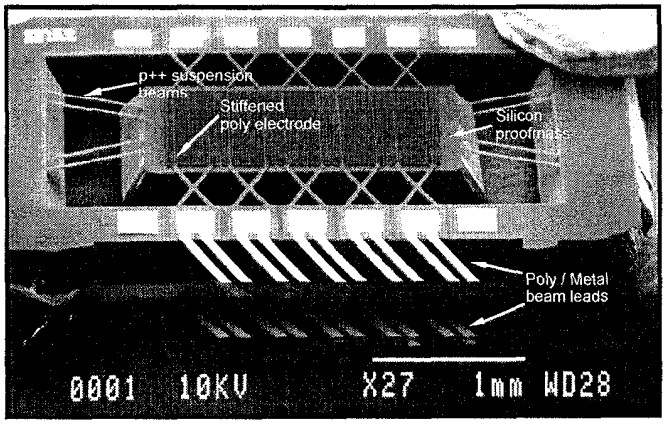

Figure 3. *SEM view of a high-precision μg accelerometer with 2mm x 1mm proofmass.*

The trenches are then refilled completely with sacrificial LPCVD oxide, LPCVD nitride and low-stress LPCVD polysilicon. The polysilicon is doped with boron at 1050°C and then annealed at 1050°C. The polysilicon is patterned to form the electrode plates with damping holes. Next 4000-5000Å LPCVD (capping) oxide is deposited. The oxide is patterned to form metal contacts and openings to bulk Si for the subsequent proofmass release. Then Cr/Au (300Å/5000Å) is evaporated and lifted-off. The proofmass is released in EDP at 110°C. The sacrificial oxide is etched in straight HF. The released structures are soaked in methanol overnight and then oven dried at 110°C.

Figure 3 shows a SEM view of the device with 2mm x 1mm proofmass. The device has 5 electrically isolated electrodes on each side, which are anchored at the rim using stiffened poly supports. Taking advantage of the selectivity of the planes in EDP, the proof mass corners have been well compensated as seen in Figure 3. Table 1 summarizes the device specifications.

Table 1. *Silicon Sensor Characteristics*

Sensor Parameters	Value
Proof Mass Size	2000 x 1000 x 450 $(\mu m)^3$
Rest Capacitance (measured)	38pF (5 Electrodes)
Sensitivity (calculated)	1.25pF/g (Bridge)
Sensitivity (measured)	1.4pF/g (Bridge)
Resonant Frequency	770Hz
Mechanical Noise Floor (calculated)	0.39μg/√Hz

INTERFACE CIRCUIT

The microaccelerometer is interfaced with capacitive readout circuitry to detect capacitance change and to operate the sensor in open-loop or force-rebalance the proof mass in closed-loop. Figure 4 shows the block diagram of the interface circuit [**6**]. Two fixed reference capacitors are used to form a full-bridge with the sensor capacitive half-bridge, and the sensor top and bottom electrodes are used as the input nodes to the chip front-end.

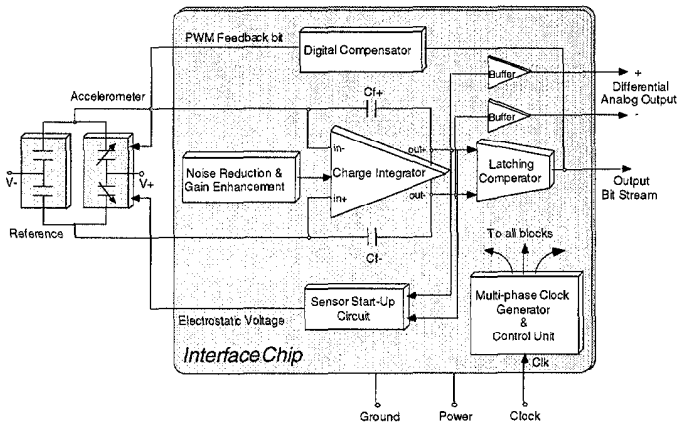

Figure 4. *Block diagram of the CMOS capacitive interface chip. The circuit is capable of both open-loop and closed-loop operation and utilizes a switched-capacitor readout technique to reduce sensitivity to parasitic capacitances [6].*

Fig. 5 shows the photograph of the circuit in 1.2μm CMOS. It has a fully-differential charge integrator with correlated double sampling to cancel 1/f noise, amplifier offset and compensate finite

amplifier gain. It utilizes digital compensation, chopping, and safe start-up to ensure high performance readout operation. It has 95dB dynamic range, a low offset of 370μV and can resolve better than 75aF/√Hz. The interface circuit has an adjustable gain in the 0.3-1.1 V/pF range. Table 2 summarizes the circuit specifications.

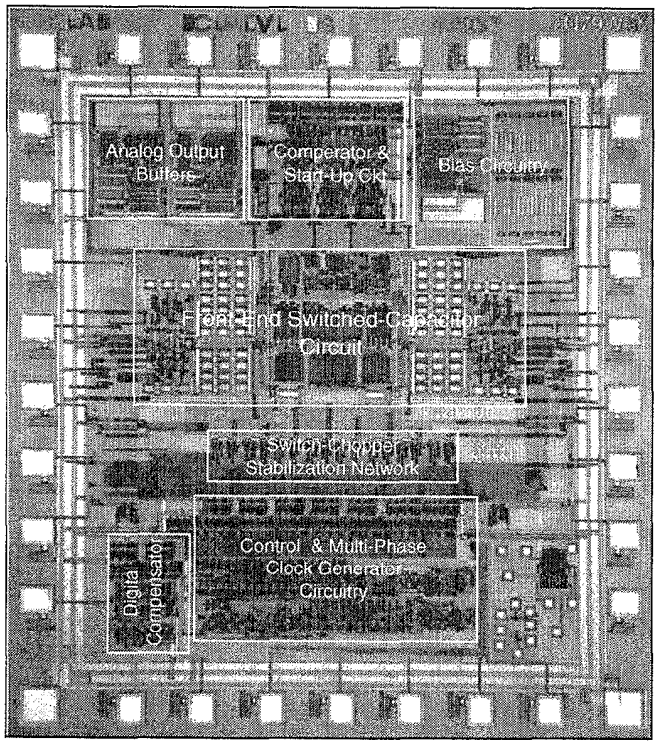

Figure. 5. *CMOS capacitive readout interface chip [6].*

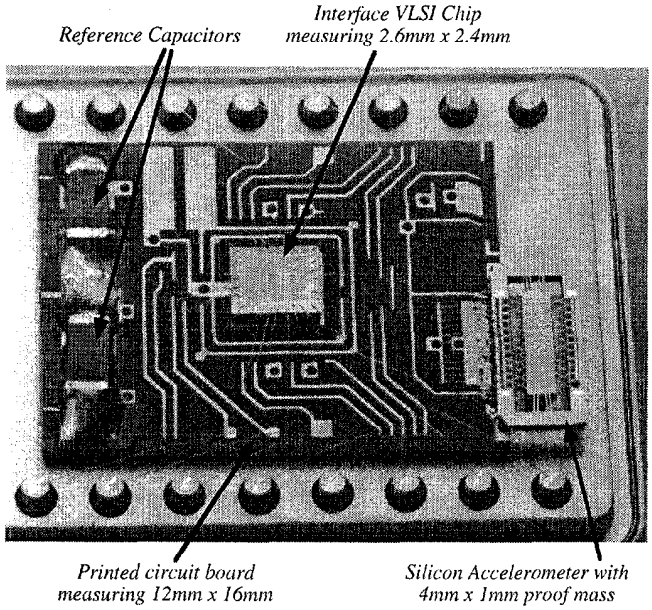

Figure 6. *Hybrid packaged accelerometer and the interface chip in a standard 24-pin IC package.*

HYBRID SUBSYSTEM-TEST & MEASUREMENTS

Figure 6 shows the hybrid subsystem with the sensor and the circuit assembled onto a PC board and mounted inside a standard DIP package. The sensor and the interface circuit are packaged close to each other to minimize parasitics. The device is mounted on the edge of the PCB to reduce any packaging induced stress.

The device (2mmx1mm) has a measured open loop sensitivity of 1.4pF/g. Figures 7 through 9 show the open-loop test results for this system. The open-loop tests were done on a dividing head, in a 1g gravitational field, by changing the acceleration on the sensor from -1g to +1g. While changing the applied acceleration, both analog output signals were measured. Figure 7 shows the results obtained from this measurement. As evident, both signals are sinusoidal and vary from 0 to 0.16 volts. The deviation from an ideal sinusoid is an artifact of the measurement setup and can be eliminated by taking a differential measurement, as shown in Figure 8.

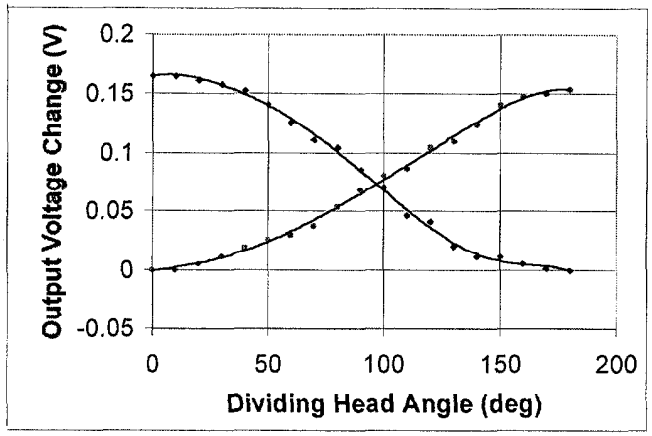

Figure 7. *Output Voltages of the sensor system for ±1g range.*

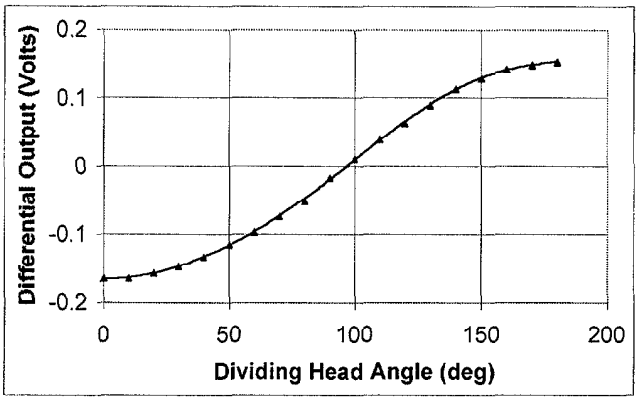

Figure 8. *Differential output voltage of the sensor system for ±1g range.*

Figure 9 shows the open-loop test results for this system with respect to acceleration indicating a sensitivity of 160mV/g. The expected sensitivity of the system (untrimmed) is ~420mV/g. The noise floor is measured using a dynamic signal analyzer HP3561. Figure 10 shows the measured output noise spectrum of the complete module with a dc input of 1g, which shows a noise floor of 3.6μV/√Hz. This indicates that the current system is capable of resolving about 20μg/√Hz. The sensitivity is lower than expected

(<3x). The reasons for this are not clear yet and are being investigated.

However, it should be noted that the circuit operates at its lower gain mode, i.e. ~300mV/pF, and hence the overall sensitivity can be increased by laser trimming the integration capacitances in the circuit. Moreover, the overall resolution can be further reduced down to sub-10μg/√Hz by using an accelerometer with higher sensitivity. For example, it can be decreased lower than 1.9μg/√Hz by using a sensor with 39pF/g sensitivity. Therefore the results obtained through the test of this hybrid-system are promising for very high resolution and higher sensitivity accelerometer systems. Temperature and shock tests have not yet been performed on these devices.

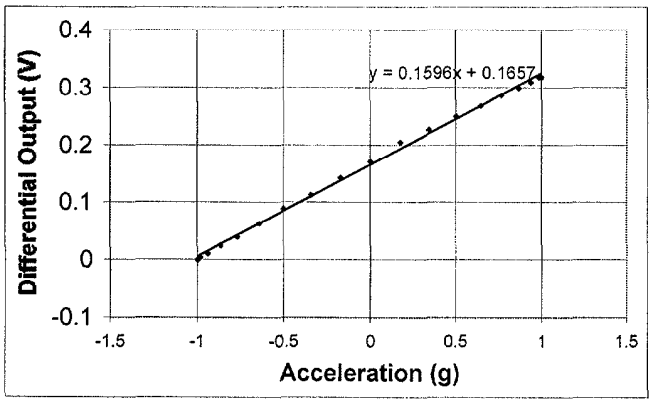

Figure 9. *Open loop test results for the sensor sub system for a device with 2mm x 1mm proof mass. The measured sensitivity is 160mV/g.*

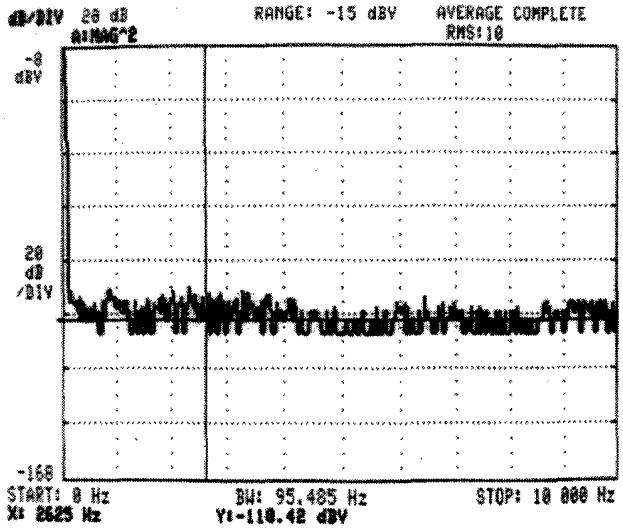

Figure 10 *Measured output spectrum of sensor/circuit module. Measured resolution of the system is ≈20μg/√Hz.*

SUMMARY

A high performance μg accelerometer with high sensitivity, low noise, and controllable damping is presented. This is achieved by combining surface and bulk micromachining and utilizes the whole wafer thickness to attain a large proof mass with integrated polysilicon electrodes. The measured sensitivity for a device with 2mm x 1mm proof mass and 1.4μm air gap is 1.4pF/g. The calculated mechanical noise floor for the device is 0.39μg/√Hz at atmosphere. The circuit has a 95dB dynamic range, a low offset of 370μV and can resolve better than 75aF. The hybrid subsystem has a noise floor of 3.6μV/√Hz and a sensitivity of 160mV/g, indicating that the current system is capable of resolving about 20μg/√Hz. Table 2 summarizes the circuit and the circuit/sensor specifications.

Table 2. *Summary of the circuit performance specifications and circuit/sensor performance*

Interface IC Parameters	**Value**
Size	2.6 x 2.4 mm^2
Sampling clock	200kHz
Power dissipation	<6.6mW @ 5V
Capacitance sensitivity	0.3-1.1V/pF (adjustable)
Noise floor	85 μV/√Hz @ 1.1V/pF
Capacitance resolution	<75 aF
Dynamic range	95dB
Offset W/o switch chopper stabilization with chopper stabilization	 2.7mV 370μV (82 ppm w.r.t. full range)
Sensor and Interface Module	**Value**
Equivalent acceleration resolution	~20μg/√Hz (measured)
Full scale range	±1.2g with 5V supply

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