MICROMACHINED STRUCTURES FABRICATED USING A WAFER-BONDED SEALED CAVITY PROCESS

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ABSTRACT

This paper discusses silicon wafer bonding technologies for the fabrication of micromechanical devices integrated monolithically with electronics. New work aimed at processes for fabrication of "surface-micromachining-like" structures such as tuning fork gyroscopes and accelerometers is described. This work provides results on a junction-isolation scheme, dry release methods to minimize stiction problems, and mechanical properties of the resultant structures. Structures fabricated using this technology for angular rate and acceleration sensing are shown. The development of these process technologies, in combination with the front-end processes previously reported, now permits full integration of electronics on silicon wafer bonded substrates in a way which provides virtually no perturbation of the IC fabrication process.

INTRODUCTION

Silicon wafer bonding has been used to fabricate surface-micromachining-like structures for a variety of sensors and actuators [1, 2, 3, 4, 5]. Recently, we proposed a method for fabrication of sensors with integrated electronics based on a silicon wafer bonding process [6]. Figure 1 illustrates the process. We begin by joining two silicon wafers, a device wafer containing an etch-stop layer and a handle wafer containing etched cavities, using wafer bonding. The bulk of the device wafer is then thinned to produce a wafer with sealed cavities which looks virtually identical to an unprocessed wafer. At this point the bonded and thinned structure can be returned to a standard IC facility for electronics fabrication. Following circuit processing, low-temperature back-end processes are performed to functionalize the sensors. The process has two significant features. First, the mechanical layer which results from this process has reliable, reproduceable mechanical properties. Second, the electronics integration strategy is compatible with standard IC processes and equipment.

Two major front-end technology issues in using wafer bonding for the fabrication of sensors and actuators; wafer thinning processes, and the control of the residual pressure in cavities formed by bonding and etchback, have been discussed in details previously [6]. In this paper, we will discuss a modification to the thinning process to achieve electrical isolation of the mechanical layer from the substrate. The back-end processes entail etching of the mechanical layer for accelerometers/gyroscopes or etching of a pressure inlet port for the pressure sensor, followed by the low-temperature bonding of a capping wafer. This paper will discuss the etching of the mechanical layer for accelerometers/gyroscopes, and the resultant mechanical properties of this layer. Processes for etching pressure inlet ports and low-temperature capping wafer bonding are the subject of current research and will be presented in the future [7].

Thinning methods are critically important in wafer bonded micromachining processes since the thickness tolerance of the mechanical parts will be defined by this step. In our previous work [6], we described an electrochemical thinning process that produces a n-type mechanical layer on a n-type substrate. However, electrical isolation is important for a class of structures built in this technology

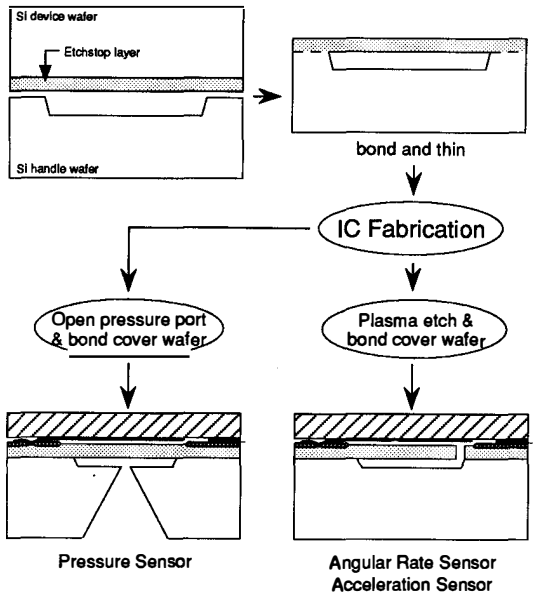

Fig. 1 MIT wafer-bonded integrated sensor process

(accelerometers and gyroscopes, for example). Two technical approaches are either to use a buried chemical etch-stop (p^{++} doping or oxide) and bonding to an oxide coated substrate wafer (*dielectric-isolation*) or to use a junction electrochemical etch-stop and a p-type substrate wafer (*junction-isolation*) as illustrated in figure 2. While the chemical etch-stop permits formation of dielectrically isolated mechanical parts, the availability, quality, and cost of either SOI starting material or buried p^{++} epi is a limiting factor. Electrochemical etch-stop methods are known to produce high quality mechanical structures, but the layers are most conveniently formed by silicon-silicon bonding, where the lower wafer provides an accessible electrical connection during the etch-stop process. This process thus precludes electrical isolation of the mechanical parts from the substrate. In an attempt to capitalize on the convenience of a silicon-silicon bonded electrochemical etch-stop, while still achieving electrical isolation of the mechanical layers, we have implemented a pnp structure for the etch-stop. This paper discusses results on the pnp electrochemical etch-stop process, and the effectiveness of the resultant junction-isolation scheme.

A second important feature of the integrated process is the ability to fabricate these parts using a completely dry release process. A resist mask is used for device patterning followed by a Si plasma etch to pattern the mechanical structure and a plasma etch to remove the resist. With this dry release method, large suspended plates have been successfully fabricated as tuning fork tines for the gyroscopes and the proof masses for the accelerometers. This paper describes this dry release process in details.

SEALED CAVITY WAFER FABRICATION

The process in figure 1 can be segmented into three sub-processes; pre-IC fabrication, IC fabrication, and post-IC

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fabrication. The IC-fabrication sub-process will not be discussed in this paper. A detailed process description for pre-IC fabrication and post-IC fabrication sub-processes is provided in the following sections.

Pre-IC Fabrication Process

The process starts with two wafers, a handle wafer containing etched cavities, and a device wafer containing the mechanical layer. In this work, three different types of device wafers were used, as summarized in table 1. The first two (diffused and epi) are used in the junction-isolation process, and the third is used for dielectric-isolation. Each of those processes is described in further detail in the following sections.

A) Junction-Isolation Process

Figure 2(a) illustrates the sealed cavity process with junction-isolation. Epi wafers were formed by growing a n-type (5 Ω-cm) layer on a p-type (10-20 Ω-cm) substrate with an average thickness of 11 μm. Diffused-junction device wafers were formed by implanting phosphorus in p-Si wafers (10-20 Ω-cm) followed by a 23-hour drive-in at 1150°C to obtain a junction depth of 10 μm.

The handle wafers are subjected to a boron blanket implant and drive-in to heavily dope the back surface (> $5x10^{19}$ cm^{-3}) in order to ensure good electrical contact during the electrochemical etch and to provide ohmic contact for backside metalization later in the fabrication process. All handle wafers contain 1–2 μm-deep trenches formed by plasma-etching.

After being hydrated with a standard RCA clean, device wafers and patterned handle wafers are contacted in a pure oxygen ambient using a single-wafer spinner with a modified Teflon chuck which can hold two wafers face-to-face, separated by Teflon shims. A detailed description on the controlled ambient bonding apparatus and procedures is provided in *reference* [6]. After the bonded wafers have been inspected for the presence of voids using an infrared camera, they are then subjected to a high temperature anneal for one hour at 1000°C in a nitrogen ambient to strengthen the bond.

Subsequently, the device wafer is thinned back using a two-step process. First, the wafer pair is ground and polished to remove about 400 μm of silicon from the device wafer. The wafer surface is chemically polished until a mirror smooth finish is obtained. The wafer pair is then electrochemically etched using the procedures and apparatus identical to those described previously [6]. The process differs from previous work due to the existance of an additional diode (diode #1 in figure 3) which is incorporated to provide electrical isolation in the final structure. The electrochemical etch, however, requires positive bias on the handle wafer, which acts to forward bias this extra diode. In its forward biased state, the diode has very little impact on the operation of the electrochemical etch. Thus the etch will still terminate at the junction formed between the n-epi (or the diffused n-Si etch-stop) and the p-type substrate (diode #2 in figure 3), and will result in an n-type mechanical layer sitting on a p-type substrate. A post-KOH clean procedure, consisting of piranha clean, HF dip, and a standard RCA clean, is then performed on the etched-back wafers before they are allowed to enter the IC fabrication line.

Table 1: Three sets of device wafers and handle wafers used in this study

	Set #1	Set #2	Set #3
Device Wafer	10 μm n-type diffused-junction	11 μm n-type epi junction	14.4 μm SOI
Handle Wafer	10-20 Ω-cm p-prime	10-20 Ω-cm p-prime	10-20 Ω-cm p-prime

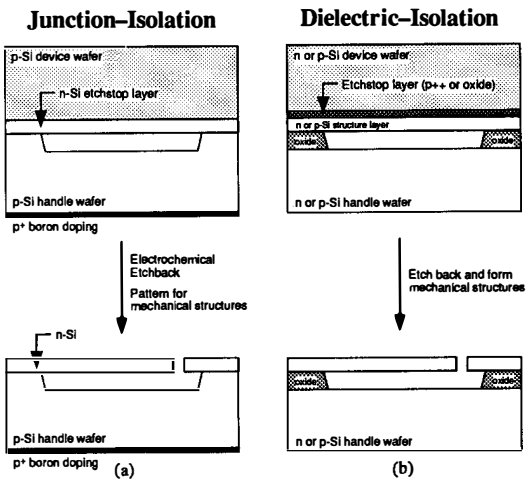


Fig. 2 Sealed cavity processes for electrical isolation of the mechanical parts from the substrate

B) Dielectric-Isolation Process

SOI wafers with 0.4 μm buried oxide, 14.35–14.42 μm-thick n-Si (6 Ω-cm) device layers, and n-Si (6 Ω-cm) substrates are used as device wafers for this process. The sealed cavity process with dielectric-isolation is illustrated in figure 2(b). The handle wafer is subjected to boron implant and drive-in as described in the previous section. Next, a layer of 1 μm-thick thermal oxide is grown on the handle wafer. This oxide layer is then patterned and etched (BOE etch) to form cavities. The backside oxide layer is protected by a resist mask during the patterning BOE etch. This oxide layer is used as a masking material during the wafer thinning process. The device wafer and handle wafer are brought to contact in a controlled ambient as described in the previous section. After initial contact, the wafer pair is then annealed for one hour at 1000°C in a nitrogen ambient to strengthen the bond.

The device wafer is then ground to remove approximately 480 μm of silicon. Next, the wafer pair is chemically etched in a 95°C, 20% (by weight) KOH solution until the etch terminates at the buried oxide etch-stop. The oxide etch-stop is then removed by wet-etching in BOE. Finally, the etched-back wafers are subjected to the post-KOH clean before they are returned to the IC fabrication line.

Post-IC Fabrication Process

As shown in figure 1, two major post-IC processing steps are required to complete the integrated sensor process; a deep Si etch to form mechanical parts, and a capping wafer process to form over electrodes [7]. The silicon etch steps will be described in detail in this section.

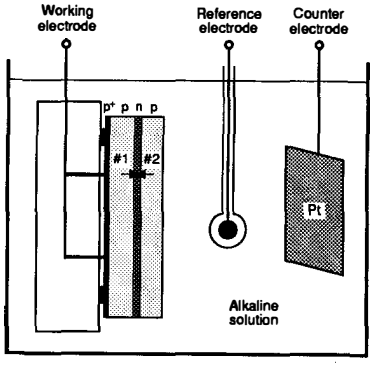


Fig. 3 Pnp electrochemical etch setup

An important feature for the wafer-bonded sealed cavity process is the ability to fabricate the mechanical parts using a completely dry release process as shown in figure 4. A resist mask is used for device patterning followed by a deep Si plasma etch (~10–15 μm) to pattern the mechanical structure. The sealed cavity has a partial vacuum and is etched at reduced pressure. Thus a differential pressure can exist accross this mechanical layer which can cause it to fail catastrophically as the etch nears completion, particularly on very fragile structures. To eliminate this problem, a two-step approach is taken in the etching process.

A 1.1 μm-thick resist mask is used to pattern "vent holes", as shown in figure 4(a), on the n-type mechanical layer. These vent holes range from 3 μm x 3 μm to 6 μm x 6 μm, and they are located at remote parts away from the devices. A 5 μm-deep Si plasma etch is used to pattern the vent holes. This is the same plasma etch chemistry which will be used to etch 10–15 μm Si later to etch free the mechanical parts. A 2 μm-thick resist mask is then used for device patterning followed by the 10–15 μm-deep Si etch (figure 4(c)-(d)). This plasma etch is based on a SF_6:CCl_4 chemistry and gives an average sidewall angle of between 83° to 86.5°, an average Si etch rate of 71.4 Å/s, and a Si:resist selectivity between 7:1 to 12.5:1 due to loading effect. The vent holes are etched through first during the deep Si etch and thus balance the pressure difference and prevent the potential "blow-out" of mechanical parts.

After the deep Si etch, the resist mask can easily be removed by an oxygen plasma. Since this is a completely dry process, no adhesion problems are observed. We routinely fabricate suspended plates as large as 1 mm by 1mm as tuning fork tines and accelerometer proof masses.

RESULTS AND DISCUSSION

A) Pnp Electrochemical Etch-stop

It is important to be able to accurately control the thickness of the bonded and etched back layer over the cavity in order to make well-defined mechanical parts. We have previously reported that the position of the "standard" np electrochemical etch-stop relative to the metallurgical junction is a function of etchant temperature, such that an increase in the temperature results in a stop closer to the junction [6].

In order to verify this temperature dependence for the pnp electrochemical etch-stop process, full wafer samples, fabricated as described above, were etched at various etchant temperatures. A cross-sectional schematic of the sample after etchback is given in figure 5. Of interest is the value of x_p, the amount of p-type silicon remaining unetched above the metallurgical junction, since if this value is zero, the thickness of the bonded layer is determined solely by the junction depth of the etch-stop layer. Spreading resistance analysis (SRA) of the etched-back wafers was done to determine x_p. Table 2 gives a summary of the results from SRA of the samples. At our usual etching temperature (95±1°C), the etch stopping point does reach the metallurgical junction. The measured roughness of the etch-stop surface is very dependent on etch-conditions, but roughnesses between 200Å and 500Å are typical.

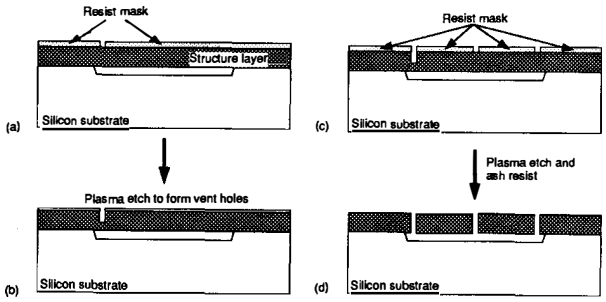


Fig. 4 Dry etch/dry release process

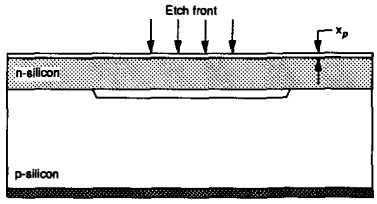


Fig. 5 Sample cross-section after electrochemical etchback

Table 2: Pnp electrochemical etch results

Etchant Temp. (°C)	x_p from SRA (μm) Set #1	Set #2
95 ± 1	0.0 + 0.1	0.0 + 0.1
90 ± 1	0.0 + 0.1	0.0 + 0.1
85 ± 1	0.4 ± 0.1	0.3 ± 0.1
75 ± 1	0.7 ± 0.1	0.5 ± 0.1

1. 10 μm diffused-junction device wafer on p-Si handle wafer
2. 11 μm n-epi device wafer on p-Si handle wafer

B) Junction-isolation Scheme

In order to evaluate the effectiveness of the junction-isolation scheme used in this study, the characteristics of diodes formed between the n-type bonded layer and the p-type substrate were measured. A total of 18 diodes per die, with variations in junction areas and perimeters, were fabricated. Figure 6 is an example of the measured I-V characteristic (n-epi sample). The diodes formed between the 10 μm diffused layer and the p-Si substrate have an average reverse-biased breakdown voltage greater than 30V and a typical current density of 0.13 pA/μm^2 at 1V reverse-bias and 2.31 pA/μm^2 at 25V reverse-bias. For the 11 μm n-epi samples, the average breakdown voltage is greater than 60V with a typical current density of 0.016 pA/μm^2 at 1V reverse-bias and 0.082 pA/μm^2 at 25V reverse-bias.

With an average operating voltage of ±2.5V, this level of reverse-bias leakage current is relatively high but acceptable. The success of this junction-isolation scheme enables us to fully utilize silicon-silicon bonding yet obtain adequate electrical isolation of the mechanical parts from the substrate.

C) Mechanical Property

Several lateral resonant structures were fabricated and tested to demonstrate the process and measure the mechanical properties. These tuning-fork-gyroscope-like lateral resonators (illustrated in figure 7) were driven to resonance by means of comb-drive. All three types of resonators have measured resonant frequencies within 5% of the FEM calculated values, as shown in table 3, using published values for the modulus of single-crystal silicon [8].

As further evidence of this, arrays of cantilevers and fixed-fixed beams were fabricated as mechanical property test structures to extract Young's Modulus and residual stress of the bonded and etched back silicon layer. Electrostatic pull-in tests were done on these test structures. The modulus determined from these measurements was consistant with published values, and the stress was zero to within the measurement resolution of 100 kPa (<10^{-6} strain). Detailed discussion on pull-in models, theories, and test results is presented in *reference* [9].

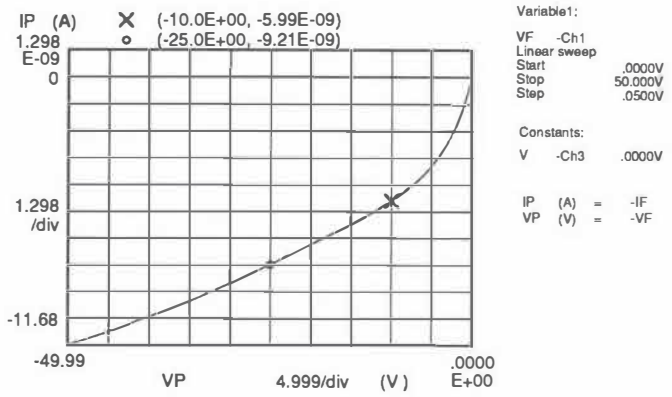


Fig. 6 A typical junction-isolation diode I-V plot

Table 3: Lateral resonator experimental results (about 6 devices per type were measured)

Device	Tine Size (μm^2)	Resonant Frequency (calculated)	Resonant Frequency (observed in vacuum)
Gyro Type 1	200 x 200	20 kHz	19,997.4 ± 0.1 Hz
Gyro Type 2	500 x 500	2 kHz	2047.5 ± 0.1 Hz
Gyro Type 3	1000 x 1000	2 kHz	1997.5 ± 0.1 Hz

Table 4: Device flatness measurement

	n-diffused	n-epi	SOI
Gyro Tines			
200 x 200 μm^2	63.2 ± 0.1 nm	< 24 nm	N/A
500 x 500 μm^2	478.6 ± 0.1 nm	< 33 nm	N/A
1 x 1 mm^2	1.158 ± 0.001 μm	< 28 nm	N/A
Proof Masses			
500 x 500 μm^2	520.2 ± 0.1 nm	< 34 nm	< 19 nm

Since we will employ a capacitive pickup detection/feedback scheme for both tuning fork gyroscopes and accelerometers, it is important to be able to fabricate ultra-flat suspended plates as tuning fork tines and accelerometer proof masses (figure 8). Plates as large as 1 mm by 1 mm have been fabricated for tines and proof masses. The flatness of the plates were measured using a Wyko Corporation's Topo-3D surface profiler [10]. Since we define "flatness" as the height difference between the center of the suspended plate and the edge of the plate, measurements of such were made on both tuning fork tines and proof masses. As discussed before, we have three different bonded layers to characterize; n-diffused, n-epi, and SOI device layers. Table 4 gives a summary of the results. Please note that there were no tuning fork tines fabricated with the SOI device layer. The values given in table 4 are average values obtained at five different dice on the wafer; center, top, bottom, left, and right respectively. We have data on a total of 6 n-diffused sample wafers (3 for tuning fork gyros and 3 for accelerometers), 2 n-epi sample wafers (1 for tuning fork gyros and 1 for accelerometers), and only one SOI sample wafer for accelerometer fabrication. All of the structures fabricated in either SOI or n-epi are flat to within the surface roughness of the sample. A warpage is clearly observable on all tuning fork tines and accelerometer proof masses fabricated on n-diffused device wafers. This "warpage" in the diffused devices is as large as 1.158 μm for the 1 mm by 1 mm tines.

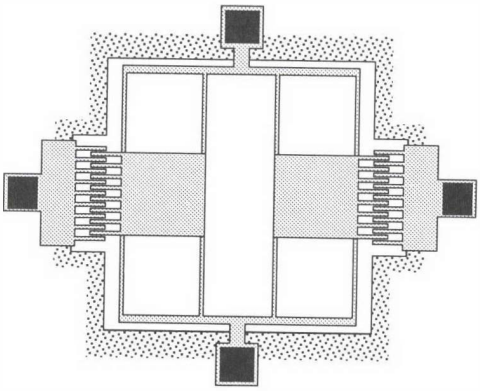
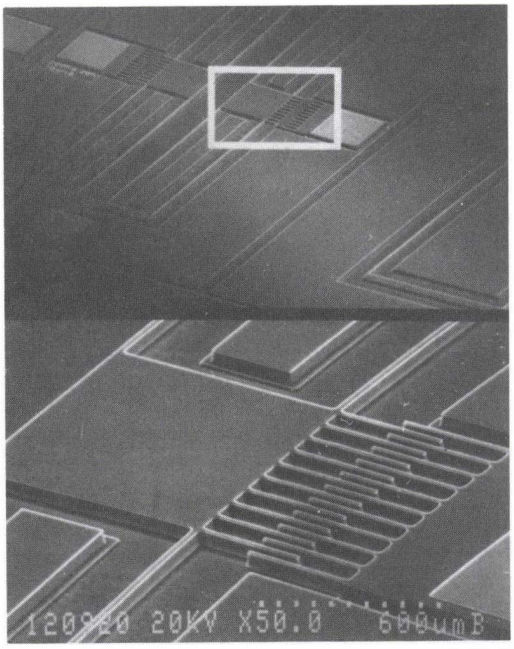


Fig. 7 Schematic and SEM photo of a tuning fork gyroscope



CONCLUSION

A stable process technology for fabrication of high quality surface micromachined structures by wafer bonding has been established. It was demonstrated that the junction-isolation scheme formed by a pnp electrochemical etch-stop process can be used to achieve electrical isolation of the mechanical parts from the substrate. It was also shown that the completed mechanical parts have excellent mechanical behavior due to a negligible residual stress in the bonded layer. Furthermore, large and ultra-flat suspended plates have been successfully fabricated using dry release methods. These processes now enable the full integration of electronics monolithically with the mechanical devices.

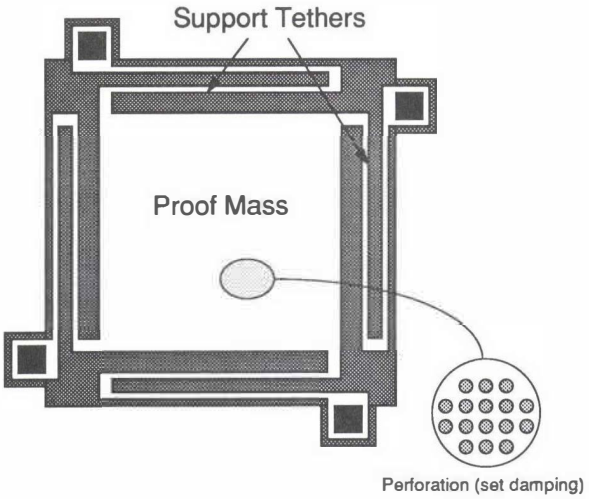
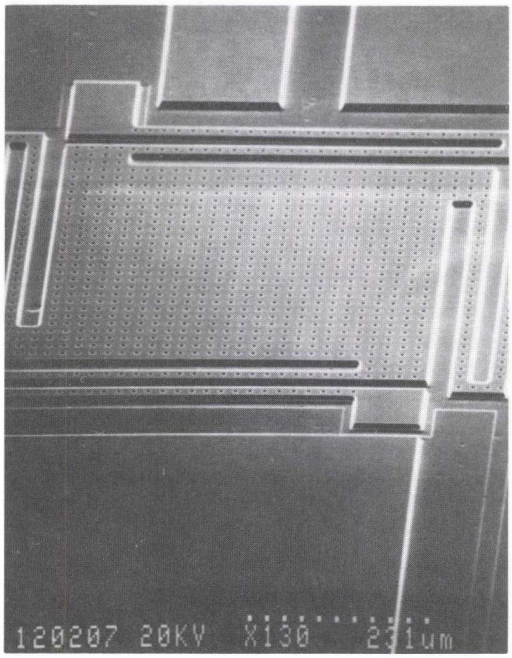


Fig. 8 Schematic and SEM photo of a microaccelerometer



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