

Silicon Wafer Bonding for Micromechanical Devices

Martin A. Schmidt
Microsystems Technology Laboratories
Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA 02139

ABSTRACT

The process for bonding silicon wafers together at high temperature is reviewed. Specific details of the bonding process as they pertain to the formation of micromechanical devices are described. Methods of characterization of the bonded wafers are discussed.

INTRODUCTION

Micromachining encompasses a broad range of technologies anchored in the core technology of microlithographic pattern transfer. A large fraction of the micromachining technologies are specific to the silicon material system principally due to the origins of the field, namely the silicon integrated circuit industry. In the silicon micromachining field, there have been two dominant fabrication methods, broadly classified as bulk micromachining (etching deep features into a wafer) and surface micromachining (depositing, patterning, and selective etching of films on a wafer). Fundamentally, both of these techniques rely on some form of etching or material removal. More recently, techniques have emerged for bonding or fusing of silicon wafers. As the bulk or surface micromachining technologies might be compared to material removal processes in conventional machining (end-milling, drilling), the wafer bonding processes are analogous to welding processes in conventional machining.

There is some potential for confusion in discussing wafer bonding processes since a wide range of processes exist. For example, the silicon-glass anodic bond is routinely used in many commercially available sensors. Additionally, low-temperature metal eutectic bonds are often used. While these bonds are quite useful in low temperature, back-end processes, they generally are not applicable as high temperature stable bonds. Thus the distinguishing feature between these methods and the bonding that we will discuss in this paper will be the ability of the bond to withstand high temperature processing without the need for intermediate layers, externally-applied pressure, or electrostatic fields to assist the bond. This bond can be performed between nearly any smooth surfaces [1-3], but generally, we will restrict our discussion to bonding of silicon wafers with or without silicon dioxide.

Interest in the process of wafer bonding as defined in the preceding paragraph was generated by the publications in 1985-86 of Lasky [4] and Shimbo [5]. Subsequently, a number of investigators have explored the use of this process for fabrication of electronic devices (SOI MOSFETs, Power Devices) [1-6]. Several commercially available electronic products exist today which employ silicon wafer bonding. Additionally, a number of investigators considered the application of wafer bonding to sensor and actuator structures. Two of the first sensors to be fabricated by wafer bonding were reported at the 1988 Solid-State Sensor and Actuator Workshop in Hilton Head [7,8]. These included a pressure sensor and an accelerometer. Since that time, a significant number of sensors and actuators have been reported which employ silicon wafer bonding. Several micromachined sensor products which use silicon wafer bonding are now available commercially.

THE BONDING PROCESS

Extensive review articles have been written on the wafer bonding process, particularly as it pertains to electronic device fabrication (1-3). This section will simply summarize the major points of the process for the bonding of silicon or silicon dioxide surfaces. The silicon wafer bonding process consists of three basic steps: surface preparation, contacting, and annealing. All of the process steps are

conducted in a cleanroom environment. The surface preparation step involves cleaning the mirror-smooth, flat surfaces of two wafers to form a hydrated surface. Following this preparation, the wafers are contacted in a clean environment by gently pressing the two surfaces together at one point. The surfaces come into contact at this point and are bound by a surface attraction of the two hydrated surfaces. A contact wave is initiated at this point and sweeps across the wafer surfaces, bringing them into intimate contact over the entire surface. The exact origin of the attractive force is not universally agreed upon [3], and depends to a certain extent on whether the bond is Si-Si or Si-SiO₂. The most common assumption is that a bond is formed between -OH groups on the opposing surfaces. The final step in the bonding process is a high temperature anneal of the contacted pair at temperatures between 800-1200C. While the room temperature contacted samples are well adhered, this anneal generally increases the bond strength by more than an order of magnitude. Measurements of the bond strength as a function of anneal temperature indicate three distinct regions. The first region, for anneal temperatures less than 300C, exhibits a relatively constant bond strength equal to the bond strength of the wafers prior to anneal. At temperatures greater than 300C, the bond strength increases and then levels out. It is presumed that a Si-O-Si bridging bond is formed between the surfaces and a water molecule is liberated. At temperatures greater than 800C, the bond strength begins to increase again. In this third region it has been suggested that surfaces can more easily deform (oxide flow) and trapped water may oxidize surfaces bringing them into better contact. At temperatures of 1000C or greater, the bond strength is in the range of the strength of the silicon crystal itself.

WAFER BONDING CHARACTERIZATION

Several non-destructive and destructive techniques exist for mechanical characterization of the bonding process. These techniques are bond imaging, cross-sectional analysis, and bond strength measurement. The imaging methods are non-destructive and can be used as in-process monitors, while the cross-sectional analysis and bond strength measurements are destructive and require control wafers for characterization.

The three dominant methods for imaging a bonded pair of silicon wafers are infrared transmission, ultrasonic, and X-ray topography. Examples of the images obtained by these methods for a poorly bonded 4" silicon wafer pair are shown in Figure 1. A simplified schematic of an infrared imaging system is shown in Figure 2. It consists of an IR source (typically an incandescent light bulb), and an IR-sensitive camera. A silicon CCD camera has sufficient sensitivity in the near-IR range that it can be used when outfitted with a filter for visible light. The bonded wafer pair is located between the source and camera. Any imperfection in the bond shows up as changes in contrast in the IR image. Large un-bonded regions ('voids') appear with a characteristic 'Newton's Rings' pattern. This imaging method generally can not image voids with a separation of surfaces less than one quarter of the wavelength of the IR source. Based on a typical particle void, this translates to a spatial resolution of several millimeter. Figure 1 clearly illustrates voids not present in the IR image which do show up in the other methods. Also, this technique works for silicon wafers of moderate doping level with smooth surfaces. Highly doped layers, IR absorbing films, or rough surfaces (backside of wafer), can limit the image quality. In spite of this resolution limit, the IR method has the advantage of being simple, fast and inexpensive. It can be used directly in the cleanroom to image the wafers before and after anneal. The other two imaging methods offer higher resolution at the expense of speed, cost and incompatibility with cleanroom processing.

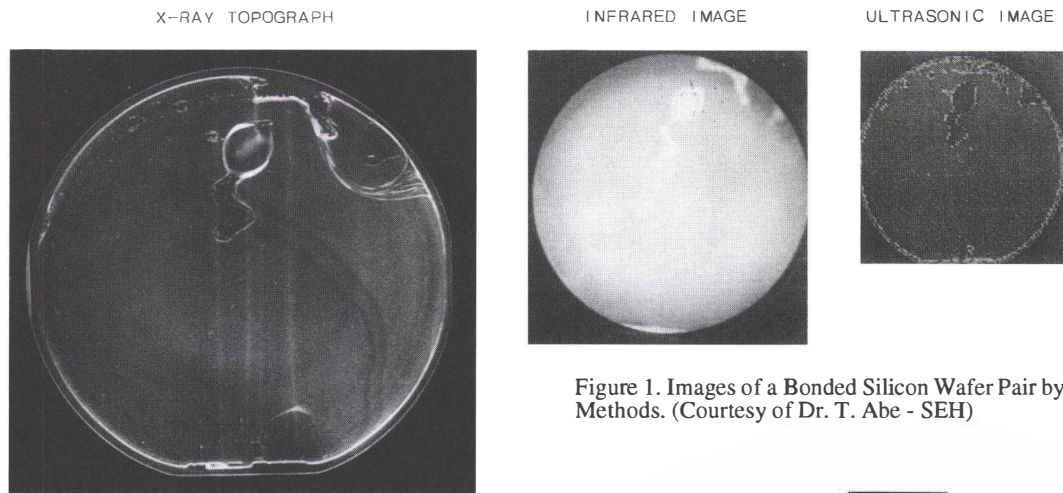


Figure 1. Images of a Bonded Silicon Wafer Pair by Several Methods. (Courtesy of Dr. T. Abe - SEH)

Cross-sectional analysis can be performed at the bonded interface by cleaving the sample. SEM and TEM techniques have been used to image the bonded interface at a submicron scale. These studies have helped to understand the composition of the bonded interface [3]. Additionally, it is possible to gain a great deal of information about the bonded interface by simply defect etching the cross-sectioned sample. Several groups have demonstrated the benefit of this approach, particularly for visualization of voids on the order of tens of microns ('microvoids') [9].

The bond strength has been characterized by a number of techniques. Figure 3 highlights the most common techniques. Pressure burst tests can often yield a number which has engineering significance in the design of sensors, but yields little information about the detailed nature of the bond due to the complicated loading of the interface. A tensile/shear test sample gives better information on the bonded interface, but is often limited by difficulties in loading and sample handling [10]. The knife-edge technique has the advantage of creating a very well defined loading on the bonded interface. A blade of defined thickness is inserted between the bonded pair in a region where a crack has been initiated. Using IR imaging methods, the length of the crack is measured, from which the surface energy can be inferred through a knowledge of the sample and blade thicknesses and the elastic properties of the wafer [11]. This method has been used with very good success. Unfortunately, the surface energy is forth power dependent on the crack length, and thus uncertainties in the crack length produce large uncertainties in the extracted surface energy. Other methods based on patterned samples have been proposed to eliminate this problem [12].

DETAILED PROCESS ISSUES

A number of factors contribute to the success of the wafer bonding process. Some of the more important details as they pertain to application in micromechanics are summarized in this section.

Starting Material and Surface Preparation

The large scale and small scale roughness of the wafer surface is very important to the success of a wafer bonding process. It is difficult to establish strict requirements on the needed wafer bow and microscale surface roughness since the surface preparation and contacting methods play a large roll. Generally, people have found that VLSI grade wafers tend to be acceptable for bonding if their microscale roughness is less than 5 Å (measured optically or by STM) and the bow is of the order of 5 μm (on a 4" wafer). Abe and Masara have done careful studies of the influence of roughness [13,14]. Protrusions and particles are sources of problems. Protrusions might be present in deposited films (epi-spikes) or be formed by processes such as oxidation of etched cavities prior to bonding [15]. Wafer polishing can be employed to minimize this problem.

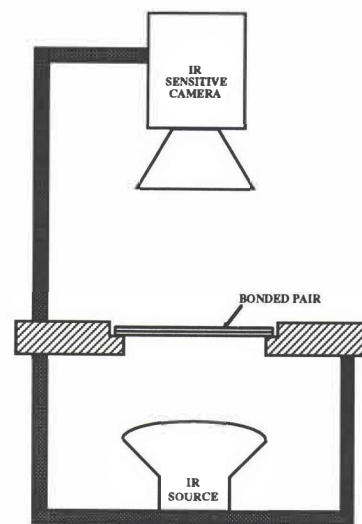


Figure 2. IR Imaging System

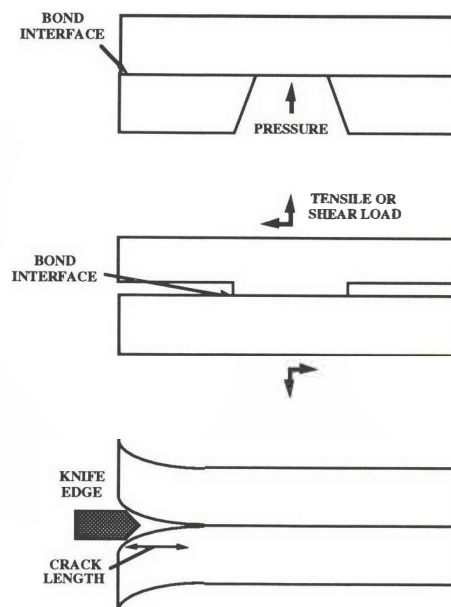


Figure 3. Examples of three bond strength measurements.

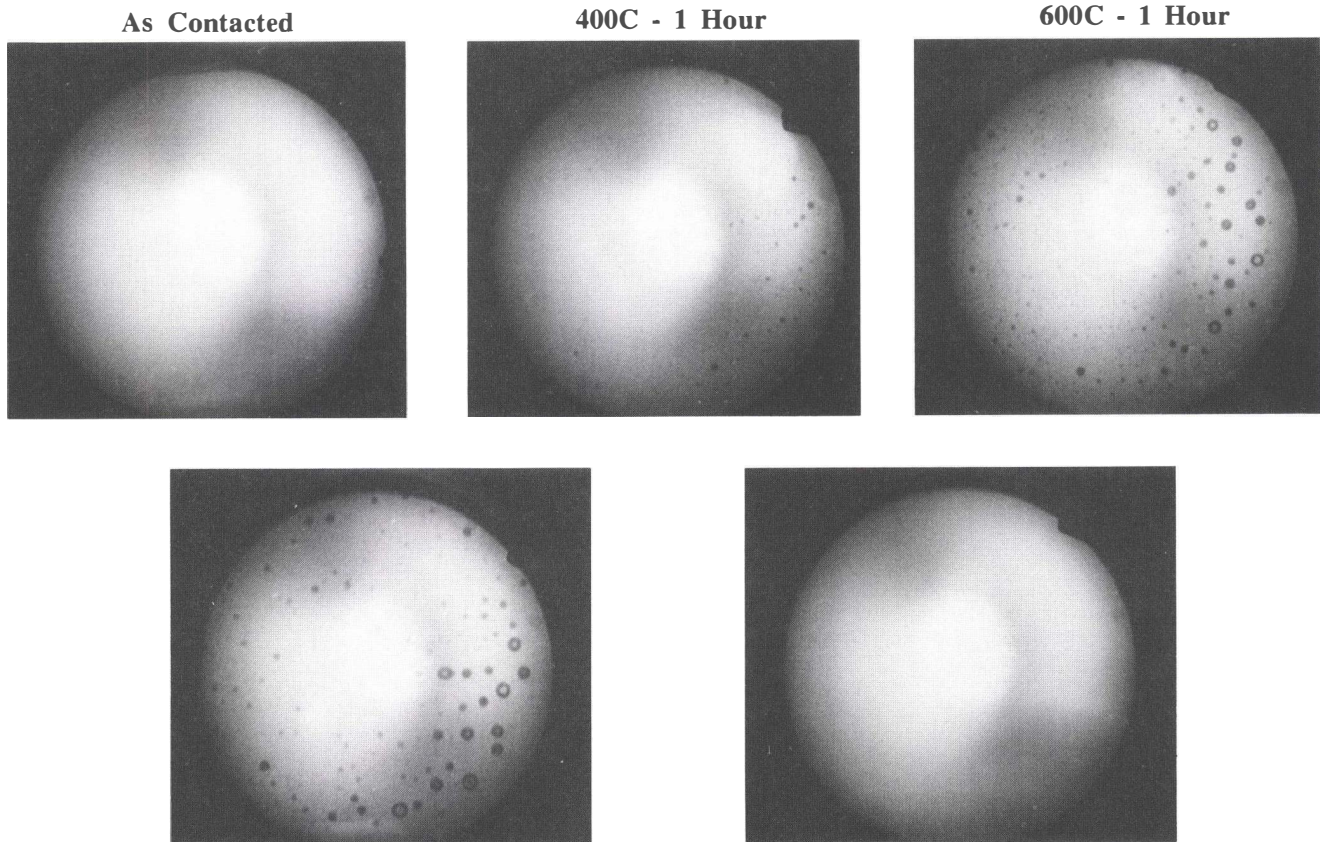


Figure 4. IR image of intrinsic voids formed in a silicon-silicon wafer bonded pair as a function of anneal temperature.

Generally, it is believed that the surface preparation should include a vigorous hydration of the surface to make it hydrophilic, followed by a de-ionized water rinse and spin dry. Processes ranging from simple water rinses to hot acid dips have been used for the hydration. However, people have also reported that HF dips, which produce a hydrophobic surface, can also be used. While the hydrophobic wafers do not contact as easily as hydrophilic wafers, there is some evidence that the final bond is better [3]. A major concern in surface preparation is hydrocarbon contamination. Exposure to plastic wafer holders has been shown to cause hydrocarbon contamination of the surfaces. These contaminants are not readily removed by standard wafer cleans, and can cause complications in the bonding as will be discussed later. Various groups have tried methods such as high temperature bakes and oxidation followed by oxide strips prior to the hydration step to minimize this problem.

Contacting

The contacting is performed immediately after the surface preparation to minimize contamination. This is done in a cleanroom, although some work has demonstrated the ability to do the bonding in a 'micro-cleanroom' [16] and under water [17]. The contact should be initiated at one point and allowed to propagate across the wafer surfaces. Contacting at multiple points can cause air pockets to be trapped between the wafers. As discussed later, in some instances it is desirable to contact the wafers in an ambient other than air, such as oxygen or vacuum. There is considerable interest in aligned bonding of wafers, and a variety of schemes have been proposed. These include the use of specialized alignment tools or mechanical fixtures which align to previously etched features in the wafer. Two common methods of mechanical alignment are to use optical fibers in v-grooves etched in the edge of the wafers, or to use reference flats on the wafers.

Annealing

In general, the highest possible anneal temperature should be used to get the best quality bond. There is very little evidence to suggest that the ambient used during the anneal has an impact on the bond quality. When processing wafers with cavities, it is important to slowly ramp the annealing temperature. Rapid temperature rises can cause the gas in the cavity to expand, building up a pressure which can separate the wafers before the bond has time to anneal. All evidence suggest that the bonding is generally complete within minutes of reaching the anneal temperature, although there is evidence that some incremental increase in bonding occurs over much longer times.

Structure of the Bonded Interface

When bonding silicon dioxide surfaces either to silicon or silicon dioxide, the bonded interface appears, based on TEM, to be nearly identical to a bulk silicon dioxide film or a thermally-grown silicon/silicon dioxide interface. Occasionally, there are small (micron-scale) voids or occlusions present. In contrast, the structure of the silicon-silicon bonded interface is very sensitive to surface preparation (hydrophobic/hydrophilic), the crystal alignment of the wafer, and the type of crystal (czochralski or float-zone). Bengtsson provides a detailed summary of the observations of this interface [3]. For hydrophilic surfaces, an interfacial SiO_x layer is observed (5-40 Å thick), but this layer can breakdown or form spheroids of SiO_x under conditions of perfect alignment of crystal planes. Preliminary evidence suggests that the hydrophobic surfaces do not have as much of an interfacial layer, which would be consistent with the removal of the native oxide layer during the HF dip used to create the hydrophobic surface.

Voids

When contacting and annealing a wafer pair, voids are sometimes observed upon inspection. These voids are generally lumped in two categories; extrinsic and intrinsic. The extrinsic voids are those created by particles, protrusions on the wafers surface, or trapped air. These voids are usually observed on contact and do not change significantly during annealing. Figure 1 shows a wafer with various forms of extrinsic voids. Intrinsic voids are voids which are generated during the anneal cycle. Figure 4 is a series of IR images of a silicon-silicon bonded pair annealed at increasing temperatures. After contact, the wafer pair appears void-free. As the anneal temperature is increased, voids begin to appear above 400C, and subsequently disappear above 900C. The voids are usually only seen when bonding silicon to silicon without an intermediate oxide and they are often attributed to hydrocarbon contamination, although there is not a consensus on their origin. It has been observed that cavities in the wafers can serve to 'getter' these microvoids, thus minimizing the problem [18].

GENERALIZED BONDING

While we have exclusively discussed bonding of silicon wafers, the same basic process steps can be applied to bonding a variety of materials. Quartz wafers can be bonded by this method [19]. Examples of bonding of dissimilar materials include the bonding of GaAs to Si [20] and Si to glass [21]. Provided the surfaces are mirror smooth and can be hydrated, the bonding proceeds in a fashion identical to Si-Si bonding. When bonding dissimilar materials, the major complication is stresses generated during the high temperature anneal due to differences in thermal coefficient of expansion of the two materials [21].

Bonding has also been demonstrated for samples with deposited films. Examples of bonding to silicon wafers with deposited polysilicon or silicon nitride have been reported [22-24]. Polishing is often needed to establish the necessary level of roughness.

BONDING WITH SEALED CAVITIES

Nearly all micromechanical applications of silicon wafer bonding require bonding of wafers with cavities etched in one or the other wafer, thus forming sealed cavities in the wafer after the bond. The nature of gases that exist in the cavities can be very important particularly in subsequent high temperature bonding. It has been shown that when wafers are contacted in air, and subsequently annealed at high temperature, the oxygen in the cavity can react with the silicon surface and create a partial vacuum (Figure 5) [25]. When the oxygen is completely consumed (for shallow cavities), the resultant pressure inside the cavity is 0.8 atm, consistent with the consumption of the 20% oxygen in air. These results indicate that the bonding process forms rapidly enough that it can trap gasses in the cavities. Under high temperatures, the residual gases trapped in the cavities can induce plastic deformation in thin silicon membranes as the gases expand [25]. This problem can be reduced or eliminated by controlling the ambient under which the wafers are contacted. We have demonstrated that the pressure inside the cavity can be reduced by bonding the wafers in an oxygen rich ambient [26]. Alternatively, it is possible to bond the wafers in a vacuum.

THINNING METHODS

Controlled wafer thinning is often a necessary process following the wafer bonding. This is particularly true in microelectronic applications such as SOI, but also in micromechanics. The two methods usually applied are precision grinding/polishing and chemical etching with etch-stops. Most of these techniques have been very effectively summarized in review articles on wafer bonding [1,2]. The precision grinding and polishing yield absolute

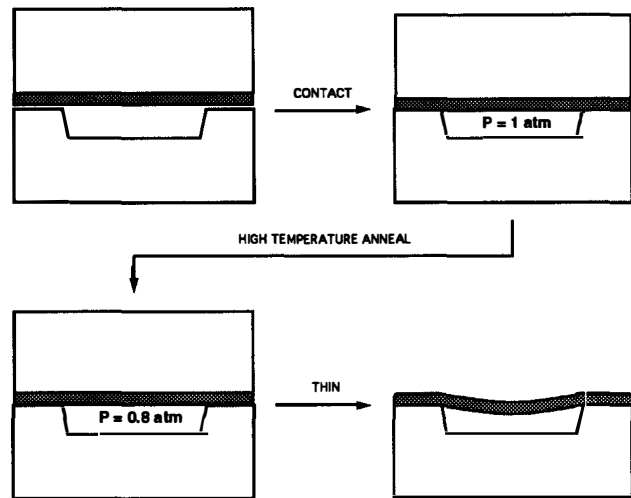


Figure 5. Sealed Cavity Formation.

thickness control between 0.25-1.0 μm . Chemical etch-stops such as the p^{++} etch-stop have also been used with good success. However, several complications result in using this process. First, the surface roughness of a p^{++} layer is sometimes too great to achieve good bonding. Second, the residual stress in the layer can produce a large wafer bow which prevents bonding. Lastly, the p^{++} layer is formed prior to bonding, and thus the bonding temperature and time must be minimized to eliminate diffusion of the layer. Counter doping the p^{++} with Ge to reduce the stress in the material can eliminate some of these problems. Electrochemical etch-stop methods have been used successfully in a number of wafer bonding applications [27]. One disadvantage of this etch-stop is that it requires complicated fixturing.

CONCLUSIONS

The wafer bonding process is an extremely powerful process for micromechanical devices. It complements other micromachining techniques by permitting the 'welding' of silicon wafers. This paper reviewed the methods for silicon wafer bonding. A detailed description of the process of wafer bonding has been described. Issues which impact the success of the wafer bonding process were identified. While a better understanding of the process is still possible, the bonding process is readily applicable in a broad range of devices.

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