

Reliability Study of Polysilicon for Microhotplates

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Abstract

Measurement results of resistance variations in thin film polycrystalline heating elements for thermally isolated microhotplate applications are presented for DC and AC conditions and different stress levels. The resistance variations observed were due solely to thermal effects arising from current-induced self-heating resulting in grain growth (recrystallization) of the polysilicon. Although the operating currents were low ($I \approx 1.5\text{mA}$, $J \approx 10^5\text{A/cm}^2$), catastrophic failure of the microhotplate was observed and this was due to microstructure damage caused by excessively high temperatures. No electromigration effects were observed.

1 Introduction

Polycrystalline silicon is widely used not only in the integrated circuit (IC) technology, but also in thermal-based microsensing applications where it serves as a heating or sensing element. Although the deposition conditions and hence, the material characteristics may be identical in both categories of applications, the long term reliability issues, in the two cases, can turn out to be significantly different in view of differences in device operation. In VLSI and related applications, variations in resistance leading to failure can be attributed to electromigration arising from very large current densities ($\approx 10^6\text{A/cm}^2$) (see [1, 2]). In thermal-based microsensors and related applications, the high thermal isolation with micromachining can result in high resistor temperatures even at low current densities ($\approx 10^5\text{A/cm}^2$), leading to significant resistance drifts (see [3, 4]).

In general, the reliability of polysilicon is governed by the electrical current density in the material and the temperature, although the latter is a function of the electrical current itself by virtue of Joule heating [1]. At relatively lower currents, the self heating of the film results in movement of grain boundaries giving rise to grain growth (recrystallization) in regions where the local temperature exceeds some critical value [5]. This leads to a decrease in the resistance of the thin film. At higher currents and with extended operation, the temperatures become significant and an increase in resistance can be observed due to thermally-induced motion (electromigration) of impurities. This gives rise to local depletion of impurities thus significantly increasing material resistivity and eventually leading to catastrophic failure [1].

In this paper, we present measurement results of polysilicon resistance variations for different stress levels and under DC and AC conditions. The measurements were performed for microhotplate test structures comprising of two meandering resistors with one acting as control. In particular, two hot plate configurations were considered; structures with and without metallization over the active area.

2 Experimental Setup

A photomicrograph of the microhotplate test structure used in the experiments is shown in Fig. 1a along with its schematic in Fig. 1b. The device was fabricated using the Northern Telecom $1.2\mu\text{m}$ CMOS process. Two symmetrical polysilicon resistors, sandwiched in oxide, with a nominal room temperature resistance of $29.9\text{k}\Omega$, meander in parallel over the hot plate as shown in Fig 1b. The resistors, denoted as R_h (heater) and R_c (control), have a $1.2\mu\text{m}$ line width and a process specified sheet resistance of $30\Omega/\square$. The sheet resistance was found to have a scatter of

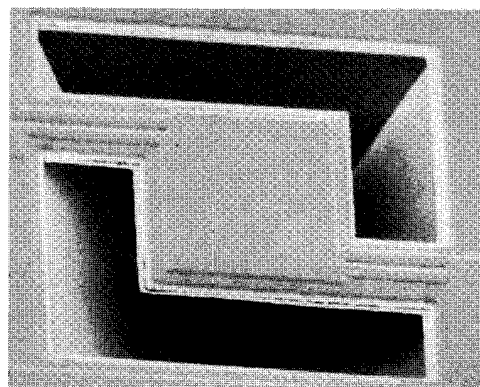


Fig. 1a - SEM of microhotplate structure used for reliability studies.

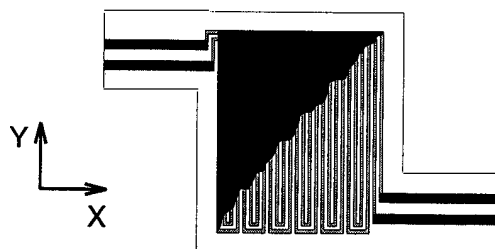


Fig. 1b - Schematic of microhotplate test structure with cut-away view showing R_h and R_c (see text).

less than 0.5 % over all samples tested. Power is supplied to the hot plate through metal lines along the support beams. The structure is underetched (micro-machined) using EDP to a depth of approximately $80\text{ }\mu\text{m}$ providing a high degree of thermal isolation from the silicon substrate. The active hot plate area (the area comprising the polysilicon resistors) is approximately $87\mu\text{m} \times 71\mu\text{m}$.

Two variations of the design are examined, one in which the active hot plate area is covered with two layers of metal (metal1 and metal2 in the CMOS process), and the other where the active area is non-metallized. Figures 2a and 2b are surface plots obtained from simulations of the hot plate temperature distribution under medium bias, with and without the temperature levelling metal layers. In these simula-

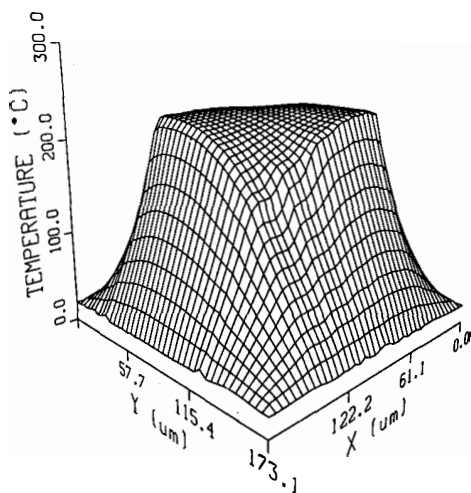


Fig. 2a - Surface temperature of hot plate under a medium bias with metallized active area.

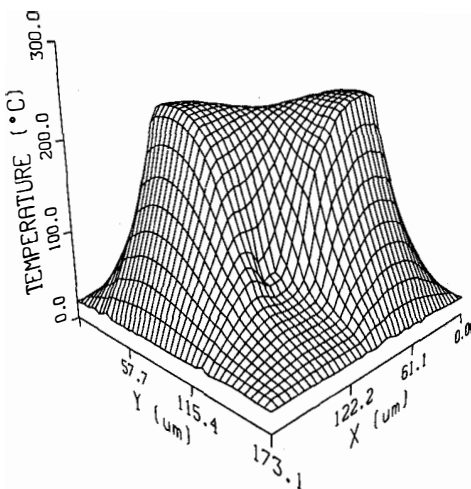


Fig. 2b - Surface temperature of hot plate under a medium bias without the metallized active area.

tions the ends of the support beams attached to the substrate were assumed equal to the substrate temperature (23°C). The additional metal layers lower the net thermal conductivity of the hot plate relative to the support beams resulting in a significantly more uniform temperature distribution over the active area. Without these layers, large temperature

gradients result near the two corners of the hot plate attached to the support beams as seen in Fig. 2b. As a consequence, a hot plate operated at the same average temperature with metallization layers, will have less severe hot spot temperatures than one operated without.

The normal operation of the test structure involves applying a high bias to R_h to heat the plate, and simultaneously a low bias to R_c . In this way, any electrically induced variations in R_h have minimal influence on R_c whose resistance changes are purely thermally induced. The tight thermal coupling obtained from the close spacing (approximately $1.6\text{ }\mu\text{m}$) of the two resistors, in addition to the minimal heat loss above and below the structure, ensures that R_h and R_c are at almost the same temperature along their entire length. In addition to R_h and R_c , a third resistor located (on the substrate) in close proximity to the hot plate is used to monitor the elevation of the substrate temperature during electrical stressing. For all experiments described in the next section, it was found that the substrate did not increase in temperature by more than 3°C . This validates the earlier assumption that the ends of the support beams at the substrate can be considered to be at room temperature; this constitutes data crucial for the boundary conditions in the numerical simulations.

All current-voltage measurements were performed at room temperature using the Keithley 236 Source Measure Units (SMU's). The SMU's can be configured to sweep a voltage or current source at precisely timed intervals, while simultaneously measuring the corresponding current or voltage. A microcomputer was used to control and retrieve data from the SMU's for the reliability studies. The resistance was constantly monitored and any changes exceeding 0.5% were recorded. In addition to the current-voltage characterisation, the temperature coefficient, α of all resistors was measured before and after stressing. The temperature coefficient, defined by $R = R_0(1 + \alpha T)$ where R_0 is the resistance at 0°C , was found to be $5.87 \times 10^{-4}/^{\circ}\text{C}$ in the range 0°C to 120°C . The measurements were performed in an oven capable of controlling the chip temperature to within 0.5°C . The temperature was measured using a thermocouple attached to the chip carrier. A low bias of $35\text{ }\mu\text{A}$ was used for the resistance measurement in order to minimise Joule heating. It was found that this bias raised the temperature of the resistor by less than 3°C . A total of 8 samples were measured with the scatter in α being less than 1%.

3 Measurements and Discussion

The current voltage characteristics of the resistor R_h of both the metallized and non-metallized hot plate structures are shown in Fig. 3. The characteristics were obtained by stepping the current through the sample with a hold time of 5 ms at each bias point. At relatively low bias, one can observe that the resistance increases with increasing voltage for both structures due to the positive temperature coefficient of the polysilicon. The heater resistances in both structures are initially similar in behaviour and

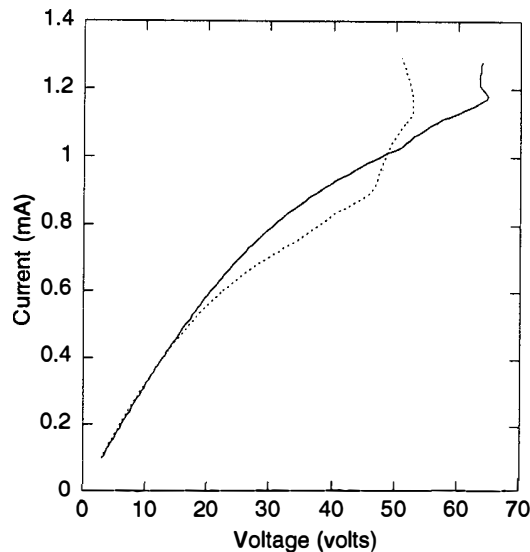


Fig. 3 - Current-voltage characteristics of heating resistor, R_h ; solid line indicates structure with metal layers over active area, dashed line denotes structure without metal layers.

the effects of nonuniform temperature start prevailing at $I > 0.5$ mA. The resistance of the metallized hot plate is lower in view of its lower peak temperatures; without the metallization, very high peak local temperatures (hot spots) are reached. In addition, there is more heat loss with the metallized structure occurring primarily through the supporting beams. At very high voltages, we note that the heater exhibits negative differential resistance (Fig. 3), similar to what was observed in [6, 7]. The increase in temperature at increasing currents leads to significant reduction in the grain boundary barrier potential possibly leading to formation of narrow filaments of molten silicon creating low resistivity paths for current flow.

The resistance of the heater and control resistors for both structures is shown in Fig. 4. We note a distinct

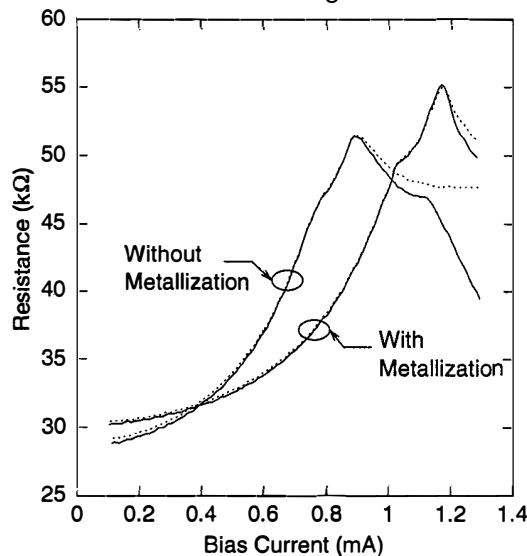


Fig. 4 - The resistance as a function of current for the same conditions as in Fig. 3. Resistors R_h and R_c are indicated by the solid and dashed lines, respectively.

kink where after the resistance decreases sharply. Under these bias conditions, the temperature of the hot plate is much in excess of 800°C . At these temperatures, there is movement of grain boundaries leading to grain growth or recrystallization [5, 8]. The subsequent increase in grain size leads to lower resistivity of the thin polycrystalline film. As expected, the recrystallization points occurs at higher voltages (currents) for the structure with metallization; more of the device active (resistor) area is at an isothermal state with a lower average temperature. One also observes a second kink after which we see a sharp decrease in the resistance. The reasons for this are not very clear but we suspect that this may be due to secondary recrystallization which takes place at much higher temperatures [5]. We also note that the control and heater resistances become increasingly more distinct as the bias current increases. This can possibly be attributed to thermally-induced variations after all, despite the close proximity of heater and the control, there are differences in temperature at the two locations.

So far, all electrical stressing of samples were based on variable but direct current (DC) conditions. Experiments were also performed for single bias DC and AC conditions to deduce the possible effects of electric fields. For the AC case, the polarity of the applied bias was switched at a frequency of 25 mHz. The measured resistances of heater and control in both microhotplate structures are shown in Fig. 5 as a function of stress times. The heater and control voltages were maintained at 35 V and 1.5 V, respectively. In these structures, the effect of heating is expected to be similar as before. No difference in the relative change in resistance ($\Delta R/R_0$) was observed between heater and the control for both structures. Here, R_0 is the respective resistance of the heater and the control, measured 1 s after the bias is applied, and ΔR is the deviation from R_0 . This indicates that the resistance variation observed is purely due to thermal effects. A direct comparison of room temperature resistance values at the start and end of a 48 hour DC

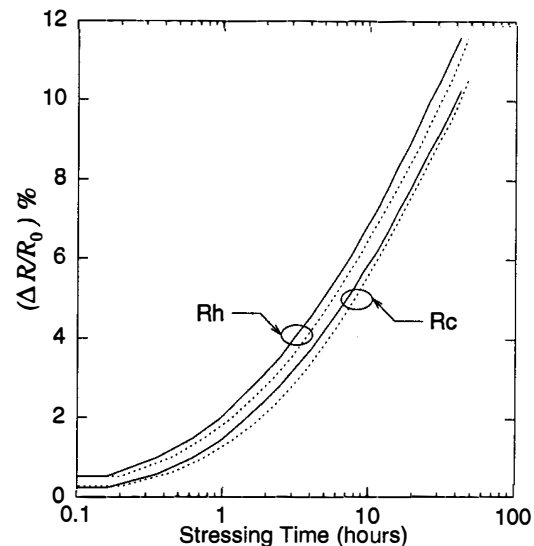


Fig. 5 - Percentage change in heater and control resistances as a function of time for a constant voltage bias. The solid and dashed lines represent DC and AC stressing, respectively (see text).

and AC stress test is shown in Tables 1a and 1b. Also included are the values of the temperature coefficient, α . No significant differences were observed between the two operating conditions. The slight discrepancy in the variation in R and α may be due to intrinsic differences in the pre-test resistance and hence, in the self-heating.

	R_h	R_c	α_h	α_s
start	29764	29968	0.585	0.584
end	35186	34660	0.513	0.585
Δ %	18.2%	15.7%	-12.3%	-17.0%

Table 1a - Heater and control resistances, and corresponding temperature coefficients, measured at room temperature at the start and end of a constant DC voltage stress test.

	R_h	R_c	α_h	α_s
start	29868	30055	0.591	0.594
end	34871	34544	0.549	0.533
Δ %	16.8 %	14.9%	-7.1%	-10.3%

Table 1b - As in Table 1a, but for AC voltage stress test.

None of the structures tested exhibited electromigration for the given range of test conditions. Unlike non-thermally isolated structures, the current densities in the structures considered had to be restricted ($J \approx 10^5 \text{ A/cm}^2$) due to excessive temperature build up as a result of thermal isolation. Electromigration, which is characterised by resistance increase, is caused by local depletion of impurities thus significantly increasing material resistivity and eventually leading to catastrophic failure. In our structures, catastrophic failure was observed only when the temperature of the active device area became high enough leading to damage of the microstructure due to mismatch in expansion coefficients and thermal melt down. In the structure with metallization, the damage occurred

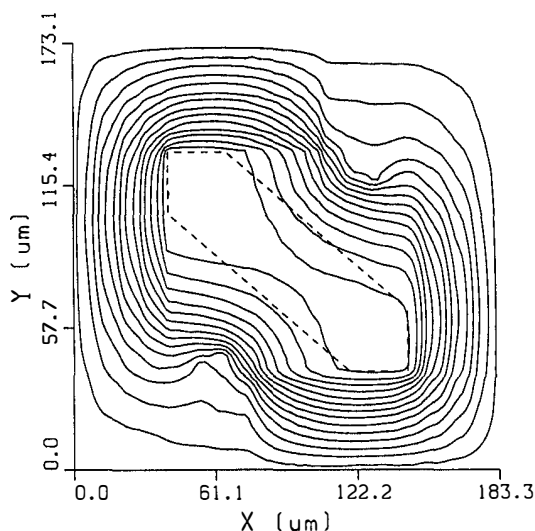


Fig. 6 - Isotherms of hot plate without metal layers under high bias. Dashed line indicates the region of catastrophic failure of polysilicon (see text).

clearly within the region indicated by dashes in the isothermal plot (Fig. 6). For all intents and purposes, this region is an isothermal surface at a temperature in excess of 900 °C. The contour lines shown are based on simulation results and the slight asymmetry is due to asymmetries in device and resistor geometry.

4 Conclusions

We have presented measurement results of resistance drifts in polysilicon heating elements in thermally isolated microhotplates. Based on measurement data obtained for long stress durations, we find that safe and reliable operation, with plate temperatures around 350°C, is possible with metallization over the active hot plate area. At this temperature, the variation in heater resistance was found to be less than 1% over 100 hours of operation.

Acknowledgements

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References

- [1] J. R. Lloyd, M. R. Polcari, and G. A. MacKenzie, "Observation of electromigration in heavily doped polycrystalline silicon thin films," *Appl. Phys. Letts.*, vol. 36, pp. 428-430, 1980.
- [2] H. Akimori, N. Owada, T. Taneoka, and H. Uda, "Reliability study of polycrystalline silicon thin film resistors used in LSI under thermal and electrical stress," in *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 276-280, 1990.
- [3] M. Parameswaran, A. M. Robinson, D. L. Blackburn, M. Gaitan, and J. Geist, "Micromachined thermal radiation emitter from a commercial CMOS process," *IEEE Electron Device Letts.*, vol. 12, pp. 57-59, 1991.
- [4] C. H. Mastrangelo, J. H. Yeh, and R. S. Muller, "Electrical and optical characteristics of vacuum-sealed polysilicon microlamps," *IEEE Trans. Electron Devices*, vol. 39, pp. 1363-1375, 1992.
- [5] C. D. Ouwers and H. Heijligers, "Recrystallization processes in polycrystalline silicon," *Appl. Phys. Letts.*, vol. 26, pp. 569-571, 1975.
- [6] D. W. Greve, "Programming mechanism of polysilicon resistor fuses," *IEEE Trans. Electron Devices*, vol. 29, pp. 719-724, 1982.
- [7] K. Ramkumar and M. Satyam, "Negative-resistance characteristics of polycrystalline silicon resistors," *J. Appl. Phys.*, vol. 62, pp. 174-176, 1987.
- [8] G. C. Jain, B. K. Das, and S. P. Bhattacharjee, "Grain growth in polycrystalline silicon," *Appl. Phys. Letts.*, vol. 33, pp. 445-446, 1978.