Navigation Grade Silicon Accelerometers With Sarificially Etched SIMOX and BESOI Structure

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ABSTRACT

This paper reports progress toward an all silicon, batch processed accelerometer designed to provide navigation grade performance (<50µg bias and <50ppm scale factor stability) and having a full scale range in excess of 100 g, or 10^8 dynamic range.

The fabrication process employs silicon on insulator (SOI) and silicon fusion bonding to make symmetrical, all Si, small gap (0.5µm – 1µm) electrostatically force balanced devices that are rugged during fabrication and released after bonding by sacrificial etch of the buried oxide layers.

INTRODUCTION

The aim of this work is the development of an all silicon high g range, navigation grade accelerometer with improved manufacturability over traditional bulk micromachined structures. In previous approaches [1], [2], a wafer of fragile cantilevered proofmasses capped on top and bottom by bonding to silicon or pyrex wafers with thin film electrodes presents difficulties during cleaning, handling, bond fixturing and alignment. Distortion of wafers during bonding causes difficulty in achieving electrostatic servoing gaps smaller than 2µm with this approach. Small gaps are needed for high g, force rebalanced operation with low voltage.

Surface micromachined structures also have not met the challenges of high g, high accuracy performance, being burdened by very low mass proofmass structures. Error forces resulting from environmentally induced changes in the electronic feedback loop offset cause the proofmass to be rebalanced against the electrostatic negative spring. The forces scaled by the small mass times acceleration forces from a low mass proofmass result in significant g errors.

Many surface micromachined accelerometers do not have symmetrical damping, mechanical suspension and electric fields in the direction normal to the wafer surface. These factors make the devices subject to vibropendulous rectification (a DC bias shift due to off axis vibration).

APPROACH

The performance and manufacturing goals reflected in the design are:

All silicon – no dissimilar materials
Low voltage, low power (5V)
Highly symmetrical structure
High motional to stray capacitance ratio
2 layer final alignment – more manufacturable

These design features are incorporated into two SOI process technologies, SIMOX and BESOI. Both designs are similar in size (5.2 x 4.6mm) and layout except that the SIMOX approach requires undercut diaphragms and flexures and are accordingly slotted to permit rapid undercutting. Both SOI silicon accelerometers are designed to be used in a force rebalanced mode with voltage controlled or charge controlled forcing [3]. The proofmass serves as the center node of a 3 terminal differential capacitor. The differential capacitance is used to sense the position between the proofmass and the other substrate, with these same surfaces also serving as rebalance electrodes.

SIMOX ACCELEROMETER

Each array of devices is fabricated from one 100mm diameter silicon wafer, ion implanted with oxygen through a mask to form a patterned buried oxide (SIMOX) followed by silicon epitaxy and dopant selective electrochemical etching to define flexures and proofmass.

The wafer is cut in half and folded on itself using silicon fusion bonding. After the two halves are aligned and bonded, access vias are anisotropically etched from the top outer surface terminating on the buried oxide. The buried oxide is etched away, forming an electrostatic forcing gap and providing freedom for the proofmass to move. Novel electrostatic guard structures have also been developed to reduce top to bottom electrode stray capacitance.

The process sequence is diagrammed in Figure 1 a–e. First, phosphorus dopant is used to produce n-type isolation regions in a p-type double-sided polished wafer.

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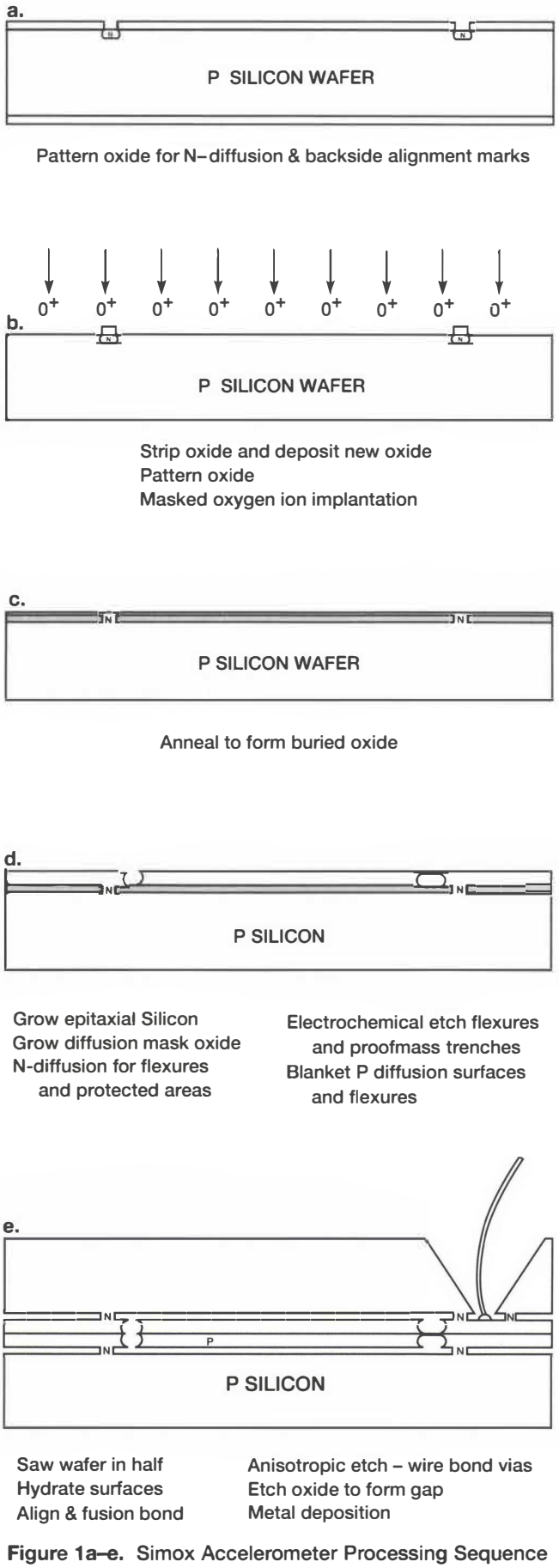

Figure 1a–e. Simox Accelerometer Processing Sequence

Next, the phosphorous masking oxide is removed and a new 800nm thick oxide is patterned over the n-type regions to mask the 200keV, 1E18/cm^2 oxygen ion implantation.

Substrate temperature is maintained above 600°C during implant to prevent surface amorphization. The wafer is then post implant annealed at over 1300°C to form a buried oxide 500nm thick beneath a single crystal silicon layer 160nm thick.

After buried oxide formation and masking oxide removal a 35μm thick, p-type silicon epitaxial layer is deposited. An n-type diffusion is patterned in regions that will later be the proofmass edges, flexure and guard structure, and grooves are KOH etched through the proofmass, stopping on the buried oxide, to control squeeze film damping.

Dopant selective electrochemical etching [4] is used to form 2μm thick undercut flexures and guard structures. The presence of a buried oxide allows overetching to eliminate the cusps that form under protected structures during this type of etching. P to N selectivities of 70-100 can be obtained if etching is carried out in darkness. Figure 2 is an SEM image of an electrochemically etched flexure. Voltage contrast highlights the n-type diffused regions.

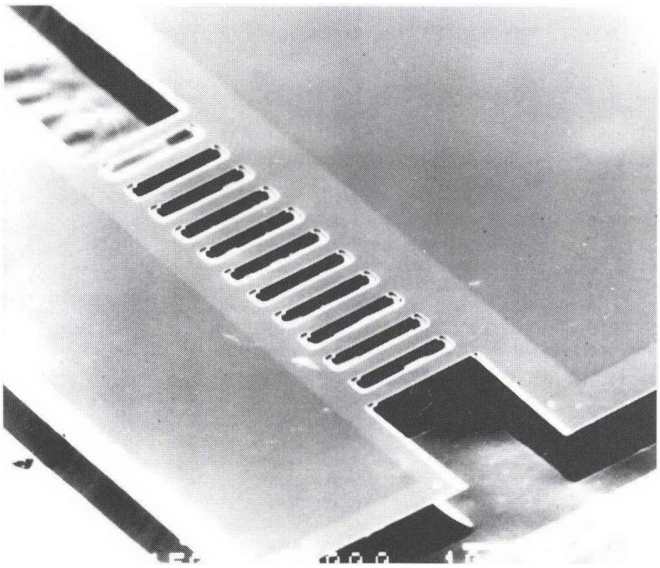

Figure 2. Electrochemically Etched Flexure

Upon completion of the electrochemical etch, the wafer is sawn in half and surfaces are cleaned and prepared for bonding with a NH_4OH-H_2O_2-H_2O solution. Infrared alignment allows the two halves to be accurately aligned and contacted. The wafer pair is annealed at 1100°C to form a strong void free bond. Topside wirebond access to all internal nodes including bottom electrode plate, guard ring, and proofmass anchor, is made through KOH etched vias etched into the top electrode plate and illustrated in cross

section in Figure 1e. The device can be released by introducing HF into these vias or as presently being done during developmental work, by dicing the wafer and performing the sacrificial etch experimentally on individual die.

The time required to sacrificially etch the buried oxide beneath the 3000μm x 3000μm proofmass has been experimentally measured to be 36 hours for a planar structure without damping grooves. The addition of damping slots should significantly shorten the undercut time but this has yet to be verified.

Single crystal silicon posts formed by the masked oxygen implant serve as the link between the outer electrode plates and the inner epitaxial silicon proofmass and guard ring frame. The single crystal posts survive long HF oxide etch times undamaged. Figure 3 is a cleaved cross section of a single crystal post bridging a 500nm gap after the buried oxide has been etched away.

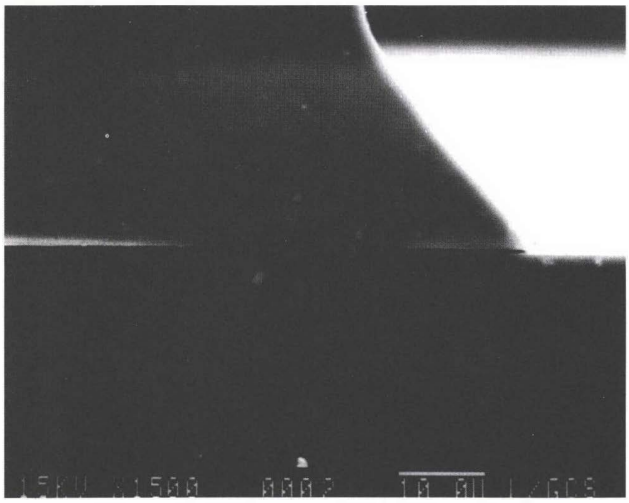

Figure 3. 500nm Gap With Silicon Post

BESOI ACCELEROMETER

Bond and etch back techniques can be used to prepare SOI wafers with another degree of flexibility. Starting with a 35μm thick silicon on insulator layer, both sides of the 35μm EPI layer can be patterned since the support substrate, or handle wafer, is background and etched away after bonding, thereby exposing the previously buried oxide as the new surface. The original SOI wafer surface is patterned with shallow damping control grooves, followed by a KOH etch outlining the proofmass and terminating on the buried oxide. Flexures are patterned while the surface topology is still flat, delayed by a protective oxide while the proofmass trench is given a head start greater than the desired flexure thickness. The gap setting sacrificial oxide is initially on the surface of another wafer and can be thermal oxide, or a faster etching CVD phosphosilicate glass. Flexure formation is simpler than the electrochemical etch used in the SIMOX case, but excellent flexure thickness uniformity (variations of a few tenths of a micron) is obtained since bulk wafer TTV does not affect flexure thickness and the epi thickness uniformity across the wafer is very good. Figure 4 is a photograph of the devices on the left and right halves of a wafer after KOH etching is completed and just prior to bonding to the sacrificial oxide wafer.

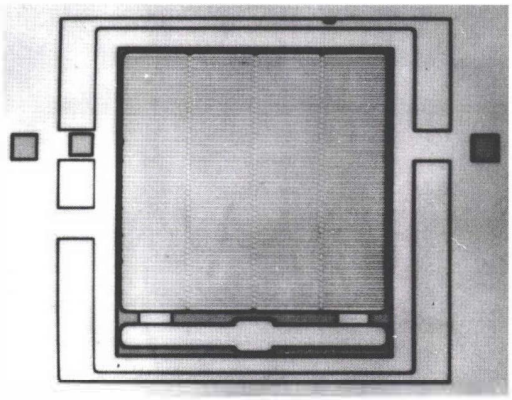

Figure 4a. Left Half of BESOI Accelerometer

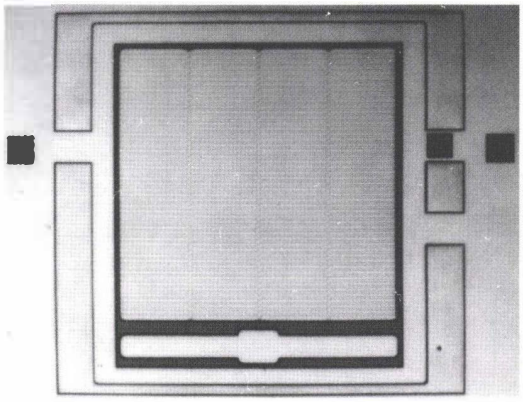

Figure 4b. Right Half of BESOI Accelerometer

After bonding these two wafers together and etchback of the handle wafer using the buried oxide as an etch stop, anchor vias are etched on the new epi surface, and bridging between the silicon epi and new substrate is accomplished with selective epitaxy. The wafer now resembles the SIMOX wafer on Figure 1d. Figure 5 is a SEM image of a cleaved BESOI wafer after the epi layer transfer. Damping control grooves are visible under the proofmass and a flexure is visible on the surface. The diaphragm visible in cross-section serves to reduce the capacitance between the substrate and guard ring.

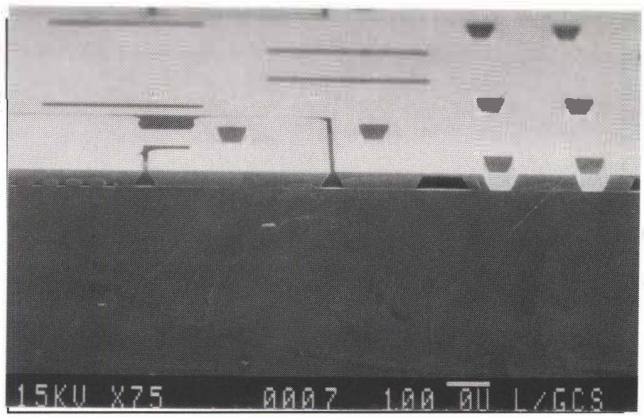

Figure 5. SEM Image of Cleaved BESOI Wafer

SUMMARY

The design and processing of symmetrical, high-g, navigation grade accelerometers presented here overcomes several performance and manufacturing limitations of prior approaches.

This new technology combining silicon fusion bonding and SOI wafers to produce sacrificially released single crystal epitaxial structures is likely to be increasingly important for fabrication of future high performance sensors and actuators, especially as the price and availability of SOI wafers continues to improve.

REFERENCES

[1] K. Warren, "Electrostatically Force-Balanced Silicon Accelerometer", Navigation, vol. 38, No. 1, pp. 91–99, Spring 1991.

[2] S. Suzuki, et.al., "Semiconductor Capacitive – Type Accelerometer with PWM Electrostatic Servo Technique", Sensors and Actuators, A21–A23, pp. 316–319, 1990.

[3] R. Stewart and K. Warren, "Force Balanced Instrument with Electrostatic Charge Control", U.S. Patent No. 5,142,921.

[4] C.J.M. Eijkel, et.al., "A New Technology for Micromachining of Silicon: Dopant Selective HF Anodic Etching for the Realization of Low Doped Monocrystalline Silicon Structures", IEEE Electron Device Letters, Vol. 11, No. 12, December 1990.