CHIP-LEVEL ENCAPSULATION OF IMPLANTABLE CMOS MICROELECTRODE ARRAYS

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ABSTRACT

This paper discusses the development of chip-level encapsulation for implantable multichannel microelectrode arrays which incorporate CMOS circuitry. The coatings must be capable of protecting the circuitry in-vivo for periods of years while maintaining selective access to recording sites having impedance levels in the megohm range. Stress-compensated, 0.75μm-thick LPCVD dielectrics provide protection over polysilicon interconnects on the electrode shanks, while 1μm of planarizing low temperature (420°C) oxide (LTO) is used over aluminum interconnect in the circuit areas. Additional layers of PECVD nitride, metal, and silicone can be added as desired over the circuit area for enhanced chemical, electrical, and optical protection. A two-step, self-aligned technique is used to define the recording sites and bonding pad areas. The resulting process allows batch fabrication of the sensors with very high yield and permits operation of both the transducers and circuitry in a challenging environment.

INTRODUCTION

An important challenge in the integration of sensors with on-chip signal processing circuitry has been providing adequate encapsulation of those circuits against the environment while providing the selective access needed between that environment and the on-chip transducers. For example, chemical sensors must typically be immersed in the analyte, and gas sensors may be required to function in the presence of corrosive gases. Implantable biosensors must operate immersed in salt water at 37°C, yet must remain robust for years since they cannot be easily replaced once implanted. One possible solution is to separate the sensors physically from the electronics; however this necessitates finding a suitable interconnect (with similar encapsulation requirements), and often results in increased packaging cost and complexity, increased size, added noise, or signal losses. Thus, it is critically important to develop chip-level packaging approaches that permit long-term circuit operation while allowing environmental access for the transducers.

An application for which such encapsulation is particularly important is the development of microelectrode arrays for recording the extracellular potentials generated by individual neurons in the central nervous system [1,2]. Such arrays are important both in studying the information processing techniques employed in biological neural networks and in the development of next-generation neural prostheses such as those for the hearing impaired. Passive recording arrays (without on-chip circuitry) have been successfully applied in many physiological studies [3,4] in both acute and chronic situations. Over 1200 of the probes developed at the University of Michigan have been supplied for such studies, and chronic implants have remained functional for periods of more than one year. These passive arrays have typically employed from 5 to 24 recording sites, but there is a growing need to integrate much larger numbers of sites into two- and three-dimensional arrays. The use of large numbers of electrodes is primarily important in allowing the user to select sites that are positioned near active neurons. Large arrays demand active electronics on the probe to allow dynamic site selection and provide signal conditioning.

Recently, thin-film recording arrays have been successfully integrated with CMOS circuitry for electronic recording site positioning, amplification of the neural signals, reduction of channel output impedances, and multiplexing of the recordings from selected sites onto a smaller number of output leads [5]. Figure 1 shows a schematic view of such an active probe. The probe substrate is defined by a region of heavily boron-diffused silicon, while the signal processing electronics are fabricated in an undoped well at the base of the probe shank. Thirty-two recording electrodes are connected to the circuitry by 3μm-pitch polysilicon interconnect lines. A photograph of a completed CMOS recording probe is shown in Fig. 2. A typical probe is 15μm thick with a shank width from 25-75μm, depending on the number of electrodes required. Shank lengths vary with the application, but are typically in the 3-4mm range.

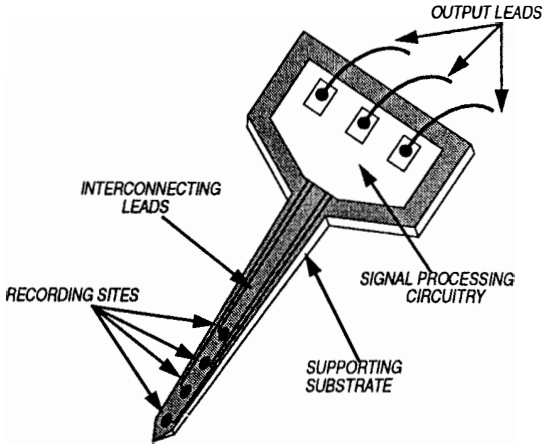

Fig. 1: Schematic drawing of a multi-site multiplexed microelectrode array.

While details of the circuit design and its measured performance have been presented previously [5,6], use of these active probes in-vivo has been limited due to low yield in producing them, which in turn has been related to difficulties in adequately encapsulating them against both the ethylene-diamene-pyrocatechol (EDP) etch used to free the probes from the substrate and the saline environment of the body. This paper presents a solution to this problem which is useful for active neural probes and which may be much more broadly applicable to integrated sensors generally.

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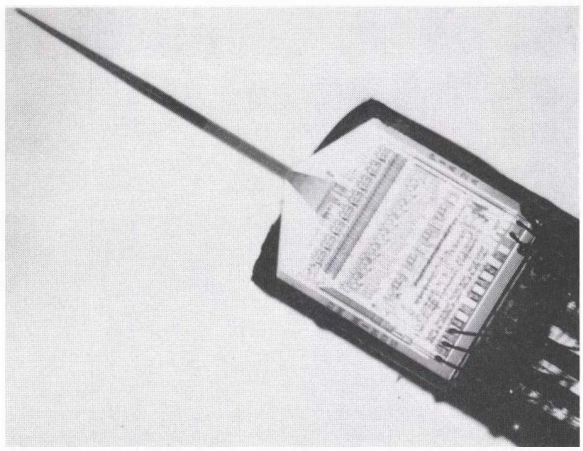

Fig. 2: Photograph of a completed 32-site micromachined CMOS recording probe.

FABRICATION TECHNIQUES

Active recording microelectrode arrays are fabricated by merging a 3μm, p-well, double-polysilicon/single-metal CMOS process with boron etch-stopped micromachining techniques [5]. First, the wafer is masked for a selective boron diffusion which defines shape of the probe substrate. Then a standard CMOS process sequence is used for the formation of the circuitry and the interconnect to the sites. Finally, the recording sites and bonding pads are defined and the probes are etched free of the substrate. A schematic cross-section of a completed microprobe is shown in Fig. 3.

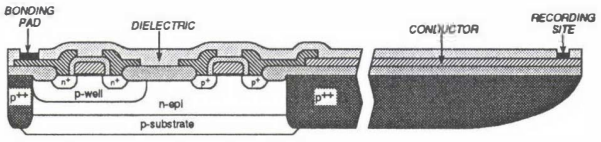

Fig. 3: Schematic cross-section of a neural probe fabricated via the merged CMOS/boron etch-stopped micromachining process.

In order to implement chip-level encapsulation for this structure, a metal-upper dielectric system is required which permits ohmic contact to the circuitry, is metallurgically stable, and yields passivation capable of protecting the sensor under bias in saline over periods of years while allowing selective access to the recording sites. We have investigated three different approaches for creating such a system: i) modification of the circuit metal to permit the use of high-temperature, low-pressure chemical vapor deposited (LPCVD) dielectrics over the entire structure prior to the final etch; ii) encapsulation with LPCVD dielectrics prior to circuit metallization, followed by the use of a noble metal for interconnect and passivation with a polymer after the final etch; and iii) use of standard aluminum circuit metallization combined with lower-temperature dielectric materials.

Refractory Metals and Silicides

LPCVD dielectrics have proven very effective in the encapsulation of passive probe structures. Such materials have permitted successful long term implants in-vivo and have maintained sub-picoampere leakage at ±5V in saline soak tests for more than three years [7]. However, their application over active circuitry demands the use of an interconnect material other than aluminum. The requirements for a circuit metal in a CMOS process are fairly rigorous: it must have very low sheet resistance and low contact resistance to both p^+ and n^+ silicon and polysilicon; it must be easy to deposit and pattern; it must have good adhesion to the encapsulating dielectrics and must have a compatible thermal expansion coefficient, and it must be able to withstand with any post-deposition chemical cleaning processes or high temperature steps. The most likely candidates for such a material are the refractory metals and their silicides, including $TiSi_2$, $MoSi_2$, WSi_2, and TiN/W. However, previously-reported approaches such as that presented in [8] have not proven feasible in this case. The finite etch rates of SiO_2 and Si_3N_4 in EDP, the need for a diffusion barrier against electrolyte penetration, the need to minimize capacitive coupling to the tissue, and the lack of circuit planarity all mandate the use of a relatively thick (>1μm) passivation layer. Additionally, it is essential that the probe shanks be flat to ease penetration and minimize tissue damage; hence, stress-balanced layers of both oxide and nitride are required over the electrode conductors. Therefore, the interconnect used must be able to withstand temperatures up to 920°C for periods of about three hours. Co-sputtered Ti/W and WSi_2 films were found to crack and peel after 20-40 minutes at these temperatures, despite the use of rapid thermal annealing (RTA) to relieve stress. Even at the minimum temperatures required for the deposition of LPCVD nitride (about 820°C) the sheet resistance of $TiSi_2$ films escalated rapidly from 2Ω/square to over 4.5Ω/square, making these films unsuitable for use in CMOS circuitry.

"Unpassivated" Metal Approach

The motivation behind the second method was the idea that if the vulnerable parts of the circuit (i.e. the silicon) could be protected from the final EDP etch with high quality dielectrics, then all that would be needed was a circuit metal which was not attacked in EDP. The circuits could then be encapsulated before implantation with a biocompatible polymer such as Dow-Corning Silastic® MDX4-4210. There are many metal combinations that are compatible with EDP, including Cr/Au, Ti/Pt/Au, and Ti/Ir. We have used all of these successfully in other applications; however, we felt this approach to be less reliable than the use of an inorganic thin film, since the sole protection for the circuitry would come from the polymer layer. This method also does not allow for the deposition of a conductive optical shield which could be grounded to the probe substrate. Accordingly, while this option could probably work successfully, we elected to pursue the method described below.

Low Temperature Dielectrics

A low stress (<100MPa, tensile), 350°C plasma-enhanced chemical vapor deposited (PECVD) nitride was developed for use over aluminum metallization; however this approach was unsuccessful due to high defect densities and inadequate step coverage in these films. In PECVD, the reaction is catalyzed in the gas phase by the plasma and there is little mobility of the reacted species once they have settled due to the low surface temperature of the wafer. We found that PECVD films were subject to minute seams around contact and metal edges (Fig. 4) which allowed EDP to attack the underlying silicon (Fig. 5). In order to obtain acceptable step coverage, it was necessary to perform several successive depositions and planarizing etch-backs. This process was both time and labor intensive and still resulted in poor yield. While PECVD films may make good inter-metal dielectrics and encapsulants for other applications, we were unable to apply them successfully to the probes, where both 1.5 hour EDP etches and long-term exposure to salt water under bias tend to reveal such problems very quickly.

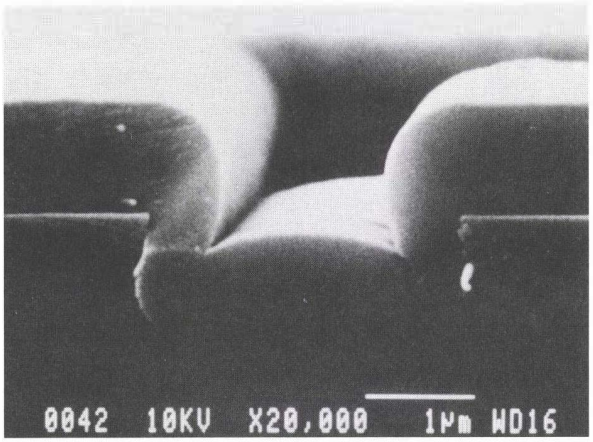

Fig. 4: Seam formed at the edge of a 1µm step by a thick PECVD nitride film.

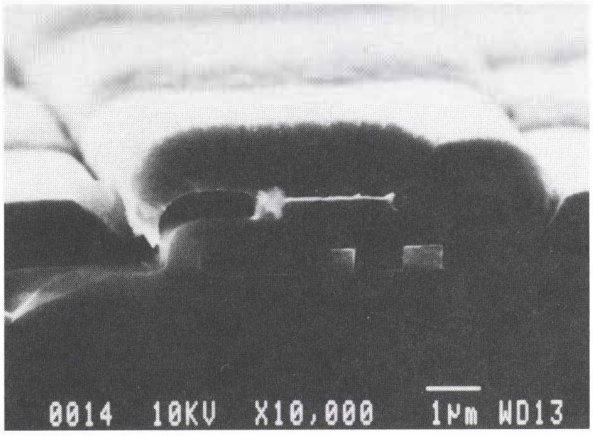

Fig. 5: Attack of the silicon substrate due to inadequate step coverage of PECVD films.

The final option investigated was the use of low temperature oxide (LTO) deposited at 420°C. Initial experiments showed that it exhibited low stress and etch rates below 500Å/hr in EDP while providing excellent coverage over step heights of 1µm as indicated by the SEM photograph in Fig. 6. A comparison of the relevant properties of LPCVD, PECVD, and LTO films is cataloged in Table 1. Several active probe wafers have been passivated with LTO and etched in EDP with no significant attack of the circuit areas.

REVISED PROCESS FLOW

Some revision of the overall probe process flow was necessary in order to incorporate LTO encapsulation. In the new process flow, electrode conductors are routed in polysilicon (instead of metal), which is deposited and patterned at the same time as the gate material so that the leads can be encapsulated by LPCVD SiO_2 and Si_3N_4. The higher resistance of the electrode conductors is not of concern here since they are connected directly to MOS inputs and draw no current. Prior to metallization, the entire probe is passivated with the LPCVD oxide/nitride combination; then contacts to the circuitry are opened. The electrode sites are opened at the same time. This is followed by deposition and patterning of aluminum metallization; however no metal is retained over the electrode sites. A thick blanket (1µm) of LTO is deposited, and then

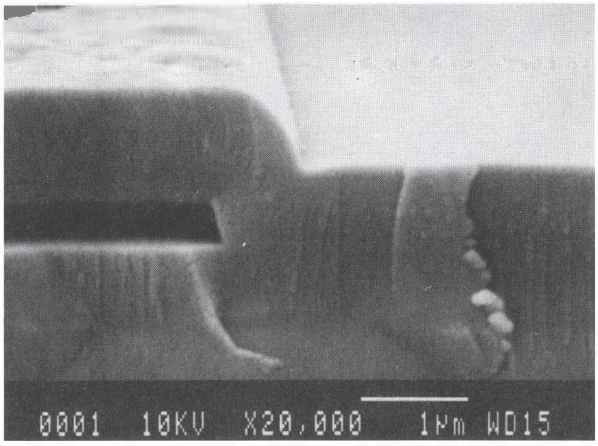

Fig. 6: Low temperature oxide (LTO) passivation of an aluminum interconnect line.

Film Type	Temp. [°C]	N_f	Stress [MPa]	BHF Etch Rate [Å/min]	EDP Etch Rate[Å/hr]
LPCVD SiO_2	920	1.460	-320	1570	300
LPCVD Si_3N_4	820	2.010	1440	<50	400
PECVD SiO_x	300	1.463	-220	3125	N/A
PECVD Si_xN_y	350	1.890	-100	280	550
LTO	420	1.455	-130	4070	485

Table 1: Comparison of measured properties of various dielectric films.

approximately 7500Å are selectively removed over the shanks and bonding pad areas. Another mask is used to remove the remaining 2500Å of LTO and inlay a noble metal (gold or iridium) in the bonding pads and sites. This two-step, self-aligned process allows contact to be made to two different materials (aluminum and polysilicon) which have two different upper dielectric structures (LPCVD + LTO or just LTO) with the same mask. Details are shown in Figs. 7 and 8. Also, PECVD nitride is frequently used on top of the LTO for additional low-temperature passivation as desired. Finally, a gold shield is placed over the circuit areas for use as an additional chemical barrier and an electrical and optical shield.

TEST RESULTS

Figure 9 shows the in-vitro response of one of the eight preamplifiers as well as the multiplexed output signal from all eight channels of one of the 32-site active probes realized with the above process. Reference "frame marks" are inserted in the 9th window of each cycle to allow external regeneration of the on-chip clock and demultiplexing of the neural signals. The probe circuitry is fully functional with high yield. Figure 10 shows single unit potentials recorded with the device in rat cerebral cortex.

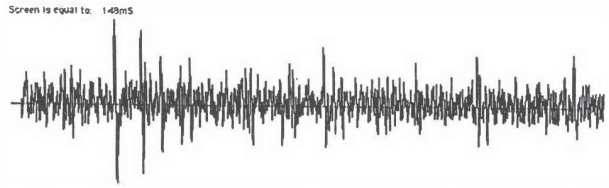

Fig. 10:Spontaneous neural activity recorded from rat cerebral cortex using a 32-site active electrode array.

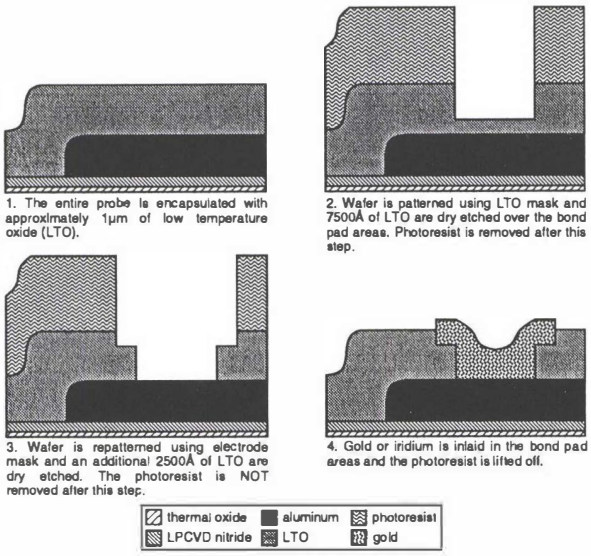

Fig. 7: Formation of bonding pads.

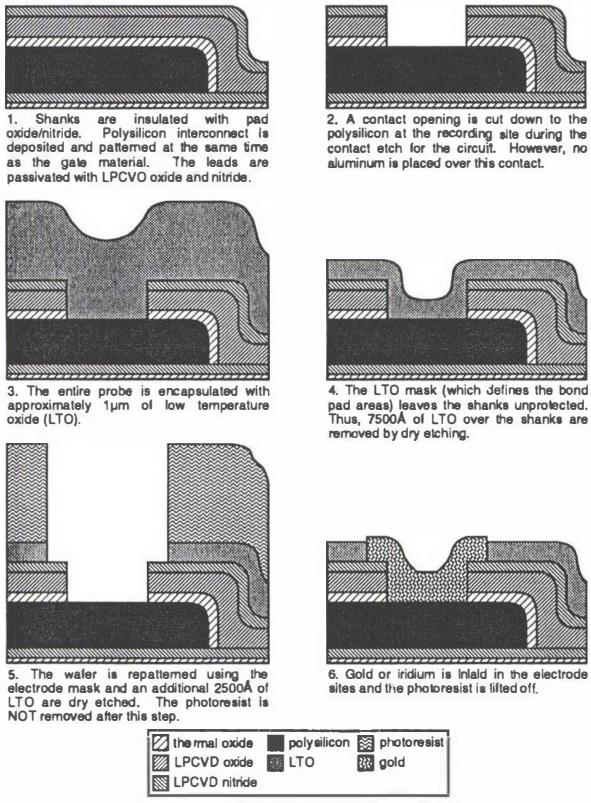

Fig. 8: Formation of recording sites.

In addition to ongoing in-vivo studies of cell localization and migration with the active probes, other in-vitro tests of this encapsulation scheme are underway. Special passive structures, similar to passive ribbon cable interconnects currently under soak, have been fabricated. These designs use aluminum interconnect and varied combinations of LTO, PECVD nitride, and gold for encapsulation. These structures are being tested for comparison of the efficacy of these films under bias in solution versus the LPCVD dielectrics used over the shanks and on passive probes.

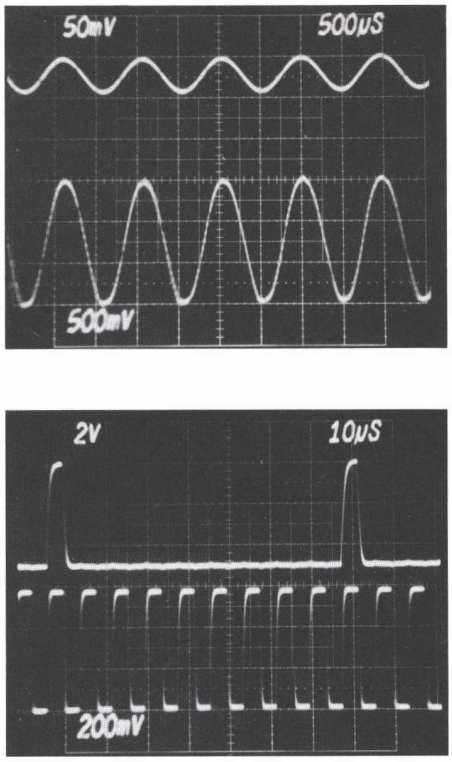

Fig. 9: Preamplifier output (top) and multiplexed data channel (bottom) from an active probe fabricated using the modified process flow.

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REFERENCES

[1] K. Drake, K. Wise, J. Farraye, D. Anderson, and S. BeMent, "Performance of Planar Multisite Microprobes in Recording Extracellular Single-Unit Intracortical Activity," *IEEE Trans. Biomed. Engr., 35*, pp. 719-732, September 1988.

[2] K. Najafi, K. Wise, and T. Mochizuki, "A High-Yield IC-Compatible Multichannel Recording Array," *IEEE Trans. Electron Devices, 32*, pp. 1206-1211, July 1985.

[3] R. Carter and J. Houk, "Multiple Single-Unit Recordings from the CNS Using Thin-Film Electrode Arrays," *IEEE Trans. Rehab. Engr.*, to be published.

[4] G. Buzsaki, Z. Horvath, R. Urioste, J. Hetke, and K. Wise, "High-Frequency Network Oscillation in the Hippocampus," *Science*, vol. 256, pp. 1025-1027, May 1992.

[5] J. Ji and K. Wise, "An Implantable CMOS Analog Signal Processor for Multiplexed Microelectrode Recording Arrays," *Digest Solid State Sensor and Actuator Workshop*, pp. 107-110, June 1990.

[6] J. Ji and K. Wise, "An Implantable CMOS Circuit Interface for Multiplexed Microelectrode Recording Arrays," *IEEE J. Solid-State Circuits, SC-26*, pp. 433-443, March 1992.

[7] J. Hetke, J. Lund, K. Najafi, K. Wise, and D. Anderson, "Silicon Ribbon Cables for Chronically-Implantable Microelectrode Arrays," *IEEE Trans. Biomed. Engr.*, to be published April 1994.

[8] W. Yun, R. Howe, and P. Gray, "Surface Micromachined, Digitally Force-Balanced Accelerometer with Integrated CMOS Detection Circuitry," *Digest Solid State Sensor and Actuator Workshop*, pp. 126-131, June 1992.