

1984

Solid-State Sensors, Actuators, and Microsystems Workshop

Greeting from the Chair

Committees

Participants

Table of Contents

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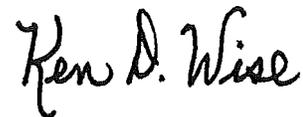
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THE 1984 IEEE SOLID-STATE SENSOR CONFERENCE

WELCOME —

On behalf of the entire Organizing Committee, let me welcome you to the 1984 IEEE Solid-State Sensor Conference and to Hilton Head Island. This Conference represents the first meeting for many years in the United States devoted primarily to sensors and may be the largest collection of sensor personnel ever assembled in this country. The enthusiasm with which you have greeted this Conference reflects both its timeliness and the rapidly growing importance of sensors in the larger scheme of solid-state electronics. Sensors now hold the keys to the successful application of microelectronics in a variety of new areas — including health care, transportation, and automated manufacturing — and as such they exercise tremendous leverage on the broader electronic field. In turn, most emerging sensors depend heavily on solid-state process technology for their formation.

This Conference will address the important application areas for sensors and the emerging technologies, structures, and circuit techniques which will make these applications possible. The Technical Program Committee has assembled a group of outstanding talks for the Conference which should serve to spark many interesting discussions. The primary emphasis at this meeting, however, is on informal interaction among those of us in the sensor field — sharing ideas, debating approaches, and simply getting better acquainted. Accordingly, the Conference depends for its success on your active participation. It is your Conference, and I hope you find it both stimulating and worthwhile.



Ken D. Wise
General Chairman



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WEDNESDAY, JUNE 6

8:30 a.m. **Introductory Remarks**

Ken D. Wise

OPPORTUNITIES FOR SOLID STATE SENSORS

Chairman: Richard S. Muller

8:40 a.m. **Solid State Sensors and Robotics**

Melvin Siegel
Carnegie-Mellon University, Pittsburgh, PA

9:20 a.m. **The Challenge of Automotive Sensors**

Joseph Giachino
Ford Motor Co., Dearborn, MI

10:00 a.m. Break

10:10 a.m. **Chemical Sensors/D.O.D.**

Ira D. Skurnick
Defense Sciences Office, DARPA, Arlington, VA

10:50 a.m. **Natural and Artificial Sensors in Neural Prosthesis**

F. T. Hambrecht
National Institute of Health, Bethesda, MD

11:30 a.m. **Microbend Fiber Optic Sensor**

Nicholas Lagakos
Naval Research Laboratory, Washington, D.C.

12:10 p.m. Lunch

SENSOR INTERFACING/ELECTRONICS

Chairman: Wen Ko

1:00 p.m. Linear ICs - A Backdoor on Sensor Technology

Paul Brokaw
Analog Devices, Limerick, Ireland

**1:40 p.m. A Micromachined Integrated Sensor With On-Chip
Self-Test Capability**

Ken Wise and Khalil Najafi
University of Michigan, Ann Arbor, MI

2:20 p.m. Sensory Inputs: Fuel for Digital Systems

Jim Knutti and Henry Allen
Transensory Devices, Inc., Fremont, CA

3:00 Break

3:10 p.m. Sensor Interface Issues: Panel Discussion

Moderator: Wen Ko

Robert Bicking, Honeywell
Paul Brokaw, Analog Devices
Janusz Bryzek, IC Sensors
Jim Knutti, Transensory Devices
Timothy Tredwell, Kodak
Ken Wise, University of Michigan

7:00 p.m. Banquet

THURSDAY, JUNE 7

SOLID STATE SENSOR STRUCTURES

Chairman: Joseph Mallon

- 8:30 a.m. **Solid State Sensor Research at Honeywell:
Active Thin-Film Plus Microstructures**
- Benjamin G. Hocker
-Honeywell Corporate Technology Center, Bloomington, MN
- 9:00 a.m. **New Dimensions for Integrated Sensors**
- Richard S. Muller
University of California, Berkeley, CA
- 9:30 a.m. **Compensation and Calibration of a Monolithic
Four-Terminal Silicon Pressure Transducer**
- C. E. Derrington, J. E. Gragg, W. E. McCulley
and W. B. Newton
Motorola, Phoenix, AZ
- 10:00 Break
- 10:10 a.m. **An Improved Monolithic Accelerometer**
- Keith Warren
InSouth Microsystems, Auburn, AL
- 10:40 a.m. **Standard Manufacturing Processes for Advanced Silicon
Sensor Families**
- Kurt Petersen and Joseph Brown
Transensory Devices, Fremont, CA
- 11:10 a.m. **Solid State Sensor Structures: Panel Discussion**
- Moderator: Joseph Mallon
- Phillip Barth, Stanford
Carl Derrington, Motorola
Benjamin Hocker, Honeywell
Richard Muller, Berkeley
Kurt Petersen, Transensory Devices
Keith Warren, InSouth
- 12:10 p.m. Lunch

SOLID STATE SENSOR ARRAYS

Chairman: Henry V. Allen

1:00 p.m. High Density Solid State Image Sensors

Timothy Tredwell
Eastman Kodak, Rochester, NY

1:40 p.m. Monolithic Silicon Fabrication Technology for Flexible Circuit and Sensor Arrays

Phillip W. Barth, Sharon L. Bernard,
and James B. Angell
Stanford University Integrated Circuit Lab,
Stanford, CA

2:20 p.m. Break

2:30 p.m. Short Talk Session (10 minute presentation on each topic)

Chairman and Organizer: J. Janata

Fabrication and Physical Sensors:

J. J. Muray, Fabrication Limits for Microsensors

H. Guckel, D. Burns and P. S. Fechner, Micromechanical Structures Formed from Polysilicon

D. L. Kendall and G. R. de Guel, Detail Control of 3D Silicon Structures Using Different Anisotropic Etching Solutions

J. Bryzek, Introducing New Concept of Sensors Interchangeability

A. G. Andreou and C. R. Westgate, The Magnetosensitivity and the Spatial Resolution of Integrated Bipolar Magnetic Field Transistors

D. E. Ioannou, A Light-Spot-Position Sensitive Photodetector

L. Harris, A Differential Magnetic Field Sensor for Position and Velocity Sensing

S. G. Joshi, Load Cell Using Surface Acoustic Waves

R. C. Hughes, FET Microsensor for Ionizing Radiation: Theory of Response and Device Characterization

Short Talk Session (continued)

Chemical Sensors:

J. H. Jerman and S. C. Terry, A Miniature Gas Chromatograph
Fabricated Using Silicon Micromachining Techniques

M. Butler, Hydrogen Sensing With an Optical Fiber Interferometer

P. K. Clifford, Fundamental Limitations of Metal Oxide Gas
Sensors

S.-C. Chang, Semiconductor Gas Sensor Technology

J. Janata, Suspended Gate Field Effect Transistor for
Gas Sensing

P. R. Barabash and R.S.C. Cobbold, Physical Origins of
Noise in ISFETs

J.H. McAlear and J.M. Wehrung, Protein/Resist Composites as
Sensing Films in CHEMFETs

8:00 p.m. Rump Session

Why Haven't Solid State Sensors Taken Over The World?

Moderator: Stephen Senturia

FRIDAY, JUNE 8

ASSORTED SOLID STATE SENSORS

Chairman: Jay N. Zemel

- 8:30 a.m. **Chemical Sensors for Vapor Detection**
 H. Wohltjen, N. L. Jarvis, A. Snow, W. Barger,
 J. Guiliani, and D. Dominguez
 Naval Research Laboratory, Washington, D.C.
- 9:00 a.m. **Basic Design Considerations for Chronically
Implantable Neural Information Sensors**
 David Edell
 Massachusetts Institute of Technology, Cambridge, MA
- 9:30 a.m. **Development of an Implantable Microdielectrometry
Sensor**
 David R. Day, Huan L. Lee
 Micromet Instruments, Cambridge, MA and
 Stephen D. Senturia
 Massachusetts Institute of Technology, Cambridge, MA
- 10:00 a.m. Break
- 10:10 a.m. **Sensor Applications of Permalloy Thin Films**
 Robert E. Bicking
 Micro Switch, Freeport, IL
- 10:40 a.m. **Electrically Actuated Micromechanical Switches
With Hysteresis**
 Paul Zavracky
 The Foxboro Company, Foxboro, MA
- 11:10 a.m. **Sensors for Biotechnical Monitoring: Panel Discussion**
 Moderator: Jay N. Zemel

 Dick Buck, University of North Carolina
 David Edell, M.I.T.
 J. Janata, University of Utah
 Stephen Senturia, M.I.T.
 Henry Wöhljten, NRL
- 12:10 p.m. Adjourn

TECHNICAL PAPERS

Solid-State Sensors, Actuators, and Microsystems Workshop

1984

**Hilton Head Island, South Carolina
June 6 - 8**

M. W. Siegel

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INTRODUCTION

The context for this paper is sensor based robotics. In contrast to the conventional hardware-based definition of robotics [1], our thinking is guided by the process-oriented definitions "a robot is a system that senses, thinks, and acts" [2] and "robotics is the application of intelligence to the control of energy and matter" [3]. Since our operational criteria specify only machine intelligence and a sensor-based window on the world, without hardware constraints, we are permitted (indeed required) to include within our purview not just machines in isolation, but also entire factories, autonomous vehicles and spacecraft, and sensor based systems for such abstractions as building environment control and energy management.

Two years ago the governing body of the C-MU Robotics Institute recognized that in the robotics community only one robot sensory modality, television camera-based imaging, was receiving systematic attention and support. They determined to do something about it by establishing the Intelligent Sensors Laboratory, and hiring physical scientists to run it. This paper summarizes some of the opportunities we have identified for ourselves as both consumers and producers of solid state sensor technology, and outlines the motivation and direction of several of our initial research projects.

THE TACTILE SENSE

The tactile sense (popularly extended to include short-range proximity sensing) is the one which, after vision, receives the greatest attention from the robotics community. Approaches to touch sensing are generally solid-state based, including microfabricated silicon devices, piezoresistive devices (especially using inhomogeneous solid suspensions, e.g., conductive particle loaded polymers), and piezoelectricity (especially using piezoelectric polymer films, e.g., polyvinylidene difluoride), and, for proximity sensing, optically coupled devices using junction semiconductor transmitters and receivers, and acoustically coupled devices using piezoelectric transducers. I will review several instances, including details of one being pursued by my student Greg Toto.

Toto has constructed a palm-like array of PVF_2 transducers mounted on the end effector of a laboratory robot. Each transducer is served by its

own buffer amplifier, ADC, and microprocessor. These perform a variety of signal-to-symbol transformations, and report compressed data through a supervisor microprocessor to an 11/750 VAX. The VAX assembles tactile world models, generates control strategies in response to them, and transmits these strategies to the robot control processor, which executes appropriate tactical moves. Our motivation is based on a timing analysis which argues that scanned tactile transducer arrays are doomed to fulfill identification roles, whereas parallel-processed transducer arrays can meet the requirements we perceive for real-time control roles. The system is presently capable of aligning the palm with arbitrarily oriented flat surfaces, and has proven useful for quantitative evaluation of heuristically based control algorithms using binary- (thresholded analog) and gray-level (full analog) tactile images.

MOBILE ROBOT NAVIGATION

Navigation of mobile robots is of interest in both structured environments (wherein the robot has prior knowledge of its workspace, and access to artificial passive and active features, e.g., retro-reflectors and transponders, for correcting dead-reckoning errors) and in unstructured environments (wherein knowledge of the workspace is learned by bootstrapping sensory information from passive features onto dead-reckoning data). Interest in the academic world is primarily on the latter mode, although practical applications in the former mode (automatic guided vehicles in the factory and office, etc.) nevertheless present opportunities for sensor development. Our institute includes two laboratories devoted to mobile robots, one (under Hans Moravec) addressing primarily vision-based methods, and the other (under Jim Crowley) addressing primarily sonar-based methods.

My student Kim Constantikes and I are working with Crowley on both improving the effectiveness of low-cost sonar devices, and on a non-imaging optical method for "coloring-in" the environmental outlines provided by sonar. We believe both of these, especially the navigation colorimeter, represent excellent opportunities for the application of silicon fabrication technology to the production of low-cost navigation aids which can effectively compete with vision systems in relatively unconstrained environments. The colorimeter uses an array of photodiodes in colors ranging from infrared to green (eventually blue) to sequentially illuminate a small

spot underneath the mobile robot, a broadband optical detector for the reflected light, and a synchronous excitation and detection scheme to develop a local color representation even in strong and strongly variable ambient illumination. The current prototype is able to distinguish among a test set of color patches, and will shortly be tried on a mobile robot.

CHEMICAL SENSING

Chemical process plants satisfy our generalized definition of robots. We furthermore postulate that the chemical process environment represents the best existing testbed for control problems in systems requiring the number of sensors and sensory modalities which will be needed by the autonomous mobile robots of the future. With this motivation, we have constructed a chemical pilot plant for investigation of sensor devices, communication and control hierarchies, and sensor based control strategies, especially those making use of the tools of the artificial intelligence community.

In coordination with this work, my colleague Paul Clifford is involved in detailed study and development of homogeneous semiconductor materials for chemical sensors. Clifford has pointed out that the chem-FET approach, using junction devices as chemical sensors, has two fundamental drawbacks: the need for "magic membranes" to achieve selectivity, and the inherent logarithmic (Nernst's Law) response of these devices. He has noted that in contrast certain homogeneous semiconductors, e.g., SnO_2 , experience resistivity changes depending on a power law rather than the logarithm of trace species concentration. His work is directed toward developing methods for predicting and controlling (by doping and chemical-physical processing techniques) the relative sensitivities of these devices to a variety of detectable species, and using computation-intensive methods to synthesize selectivity by taking advantage of systematically induced small differences in an integrated array of inherently similar devices.

OPPORTUNITIES FOR CONFIGURATION, PATH, AND COLLISION AVOIDANCE SENSING

Approaches to determining robot configuration and path, and to avoiding collisions with other robots and objects in the work environment, are commonly open loop computations, but from our perspective a sensor based approach is the only acceptable long range alternative. Our goal is to make the present requirement for mechanically rigid and precise robots obsolete: the ideal manipulator should be lightweight and "sloppy"; coping with mechanical uncertainties and load-induced flexing through sensor based learning and real-time control. Opportunities the solid state sensor community can potentially address include, in addition to the obvious proximity and tactile sensing, strain gauging, angular position encoding, three dimensional location of robot points in the coordinate system of the work, and velocity, acceleration, and

force gauging for dynamic control. Additional opportunities relate to sensing modalities for robustly insuring human safety in workplaces where people and robots might productively work together.

INTELLIGENT SENSORS IN THE ROBOTIC CONTEXT

Sensor based robotics will demand large numbers of very small, very inexpensive sensors. Because these sensors will be coupled (and in many cases eventually integrated) with local microprocessors, and will function embedded in intelligent control systems, it is rarely necessary that they be linearized or precisely calibrated. As long as they have adequate resolution, dynamic range, and stability, the systems will be able (as humans are able) to calibrate themselves. We believe that, in this context, 100 one-dollar sensors will almost always prove more useful and instructive than one 100-dollar sensor.

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Introduction

The development of low cost, reliable sensors is critical to insure the successful, broad application of automotive electronic control and monitoring systems. This application of electronics has been driven in part by government regulations and in ever increasing part by market desires for new and improved product. The engineering challenge is to develop a sensor with laboratory precision, military reliability, and hostile environment capabilities at consumer prices with an ever increasing variety of applications.

Silicon microelectronic technology must continue to be adapted to sensor needs if the technical community is to meet the demands of the future. The status of today's automotive sensors and the tasks for the future can best be understood by examining sensor applications, current sensor status, and sensor challenges.

Sensor Applications and Considerations

Currently, sensors are being utilized in the engine control, vehicle control and instrumentation areas. The number of sensors used on each vehicle depends upon model and options. The following discussion will provide a brief background as to why electronics and sensors are being applied to these three areas.

Engine Controls

The major impetus behind the application of electronics and sensors for engine control has been:

- . Government legislation
- . Fuel economy
- . Vehicle performance

In 1983, Ford Motor Company has introduced the fourth generation Electronic Engine Control System. This EEC-IV system features the first automotive 16 bit microprocessor and the speed to execute 12,500 commands during one engine revolution. The EEC-IV system can be configured to use nine sensors. The sensed parameters are:

- . Manifold/barometric pressure
- . Manifold charge temperature
- . Engine coolant temperature
- . Throttle position
- . Exhaust gas valve position
- . Piston position
- . Exhaust gas oxygen
- . Airflow
- . Engine knock

Vehicle Controls

The two major vehicle control systems in production are vehicle speed control and electronic air suspension. The speed control system uses a vehicle speed sensor and a throttle position sensor. The

vehicle speed sensor is the key element in the system's major control loop while the position sensor is used in secondary control loop to eliminate speed regulation hunting.

The electronic air suspension system contains three height sensors to determine and control vehicle height and attitude.

Current Sensor Status

Sensors used in Ford products can be grouped into the following generic categories.

<u>Sensors</u>	<u>Technology</u>
. Pressure (absolute)	Capacitance (silicon)
. Exhaust gas oxygen	Voltaic (ceramic)
. Position	Variable reluctance, Hall effect, resistive
. Temperature	Resistive
. Speed	Reluctance and optical
. Liquid level	Resistive

Each sensor and application, while an integral system component, has unique performance, package and functional requirements. The one common requirement that automotive sensors share is that they must survive in a harsh underhood environment for at least 50,000 miles (or 2,000 hours).

This environment can produce temperatures from -40 degrees C to 150 degrees C, vibrations up to 15g, mechanical shock to 50g, thermal shock, immersion or contamination with a host of fluids including brake fluid, oil, ethylene glycol and salt spray.

Each sensor and its technology will be discussed with emphasis on key requirements and fundamental design approaches.

Future Sensor Needs

The motivating forces and direction for new sensors are:

- . Lower sensor cost
- . More reliable sensors
- . Improved sensor capabilities
- . New application requirements

Sensor Costs

The key to meeting the need for reduced cost is to concurrently develop sensor designs and manufacturing techniques that allow mass production. Silicon microelectronic technology is ideally suited to this requirement.

Sensor Reliability

Long-term reliability must be designed in initially and maintained in manufacture by strict process control. Reliability cannot be tested into the sensor. The manufacturing process is as an important a product as the sensor hardware.

Improved Sensor Capabilities

Sensors will have to be designed to contain greater interfacing capabilities with electronic control modules, self-calibration, self-diagnostics and electromagnetic interference immunity (EMI). In many cases, this can only be accomplished with "smart" sensors.

New Applications

Additional opportunities for new sensors are developing as part of new system requirements. These new systems include electronic transmission control, fiber optic harnesses, as well as enhanced engine control and vehicle control systems.

Conclusions

Major opportunities exist in the worldwide automotive sensor business for lower cost, more reliable sensors. The demand is being stimulated by market pressures for new features and worldwide government requirements and regulations. Silicon microtechnology is the key technology in providing the features and functions required for the 1990's.

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Contained within the human hand and the forearm muscles that control the hand are thousands of miniature sensors. When a normal individual grasps an object, these transducers send information to the spinal cord and to the brain about the temperature, texture and weight of the object, about where the object is in space, the distribution of grasp pressure across the surface of the hand, and sometimes pain producing characteristics. If the spinal cord is interrupted in the neck, these sensory signals are interrupted along with the motor signals that normally control the muscles. Currently, research groups throughout the world are attempting to restore lost function to neurologically disabled individuals, and the devices they develop are known as neural prostheses. Functional electrical stimulation (FES) is the technique of utilizing electrical stimulation to activate excitable tissue and functional neuromuscular stimulation (FNS) is the specific term used to designate electrical activation of paralyzed muscles.

Neural prostheses can be used to transfer information into or out of the nervous system. An example of a neural prosthesis that involves inward information transfer is the cochlear implant for the sensory deaf. These individuals have lost the transducers that convert the pressure variations of the acoustic environment to the electrical signals that are utilized by the auditory nerve between the inner ear and the brain. Current cochlear implants utilize one or more electrodes implanted in the middle or inner ear to electrically activate auditory nerve fibers. The electrodes are connected to electronic circuits that include a microphone, speech processing circuitry, and appropriate stimulus waveform generators.

Another class of neural prostheses are being developed to assist in evacuation of the urinary bladder. Certain individuals with lesions of the brain or spinal cord lose the ability to voluntarily evacuate the bladder. This is not only a psychological and social problem but also can result in life threatening infections of the urinary system. Many of these individuals lose not only the ability to activate the detrusor muscle that contracts the bladder, but they also are unable to sense when the bladder is full. The sensors in the bladder are essentially pressure transducers with variable thresholds. If the bladder is slowly distended, the transducer threshold is high and the bladder can hold a greater volume before signals of discomfort are generated and sent to the central nervous system. However, if the bladder is rapidly distended, the transducer threshold is low and the message to empty the bladder is transmitted despite relatively low bladder volumes.

Ideally, a bladder evacuation prosthesis would derive bladder pressure signals from the natural bladder transducers. At the present time, this is not possible. The sensory nerve fibers from the bladder are very fine, and it is extremely difficult to detect the microvolt level signals that accompany their activation. In lieu of utilizing the natural transducers, an artificial bladder pressure transducer is needed. This implantable transducer should detect the differential pressure across the bladder wall (i.e., between the bladder interior and the abdominal cavity). It should be able to detect pressures as low as 5cm H₂O and as high as 120cm H₂O (1). The design and packaging must be such that the transducer is not affected by the saline environment or by the 100-500 micron thick fibrous encapsulation that occurs around implants. It is conceivable that the implanted transducer might include circuitry to determine the rate of increase of bladder pressure, but such signal processing is probably more easily accomplished after the basic transducer signal has been transmitted outside of the body. The simplest method of removing the signal is by direct wires with percutaneous connectors. However, these connectors can serve as an entrance route for pathogens with subsequent infections. Safer techniques include interrogation of transducer status by techniques such as grid dip oscillators or active inductive or electromagnetic transmission from the transducer.

The challenges in developing methods of activating paralyzed limbs in quadriplegic and paraplegic individuals have similarities to the bladder evacuation problems but are much more complex. People who have sustained spinal cord injuries in their necks are generally left with little or no motor control of their hands, trunks or legs, and little or no sensation in these parts. The feasibility of using FNS to activate their paralyzed hand muscles has been demonstrated in a clinical laboratory environment but not in everyday living outside of the hospital (2). Microprocessor controlled, multichannel stimulators have been developed. These take care of the bookkeeping requirements of selecting the order in which muscles are to be activated and the stimulus parameters after the paralyzed individual has specified the type and degree of motion desired. Transducers that detect voluntary contractions of nonparalyzed muscles or the position of nonparalyzed body parts are used for the derivation of the voluntary control signals. Except for visual feedback about the position of the hand, the system is essentially open loop.

This makes control rather slow and tedious as corrections must be made for non-linear relationships between muscle force output and stimulus levels, muscle length and muscle fatigue. The users must concentrate on a task rather than use their visual system to periodically sample the status as normal individuals do.

It is tempting to consider methods of making connections with the natural sensors in the skin, joints, and muscles of paralyzed individuals since these sensors are intact and are sending signals to the injured spinal cord. Under laboratory conditions in which upper extremity movement is restrained, fine wire electrodes have been introduced into human nerve trunks and signals from most of the types of transducers in the hand have been detected (3). It has not been possible to chronically record from these nerve trunks under unrestrained conditions. However, Loeb and his colleagues have developed a technique for recording from the rather large cell bodies of cat sensory neurons in the dorsal root ganglia for periods of several months (4). At this location, the relative movement of the neurons with respect to the surrounding tissues is reduced and the extracellular signals generated by the large cells are easier to record. It is conceivable that this technique might some day be developed to the point where it could be utilized in a FNS system.

Without the ability to tap the natural sensors, artificial transducers are being explored. It is the consensus of control engineers working with FNS for restoration of hand grasp that finger position relative to the thumb and the force on the grasping surface of the thumb are the two most important pieces of information needed. One concept is to incorporate transducers into a glove as illustrated in figure 1.

The original idea was to use a flexible piezoelectric polymer such as polyvinylidene fluoride (PVF₂) for both position and force measurements. Attempts to utilize the polymer as part of an ultrasonic ranging system for position measurements were defeated by the inability to achieve usable signal to noise ratios and by the fact that grasped objects block the ultrasonic signal. However, the possibility still exists of using the PVF₂ to measure force.

Firm specifications for hand position and force transducers have not been established, but tentative values for laboratory evaluation of closed loop control systems are given in Table I. Transducers based on differential transformers for position measurements and strain gauges for force measurements have been fabricated to these specifications and are now being tested. However, they are not miniature and cosmetically acceptable nor have they been designed to be durable enough to withstand the abuse that they will incur in the home environment.

It is anticipated that future FNS systems will be totally implanted. If they are closed loop systems and if suitable methods cannot be developed to tap the natural sensors, then artificial implantable transducers will need to be developed. Walmsley and Loeb have designed and tested implantable tendon tension and joint position transducers in cats (4). Although these transducers have a lifetime of several months, transducers for use in FNS systems must have much longer lifetimes and must be able to detect the force distribution across the grasping surfaces. To the author's knowledge, no attempt has been made to do this with implanted artificial transducers.

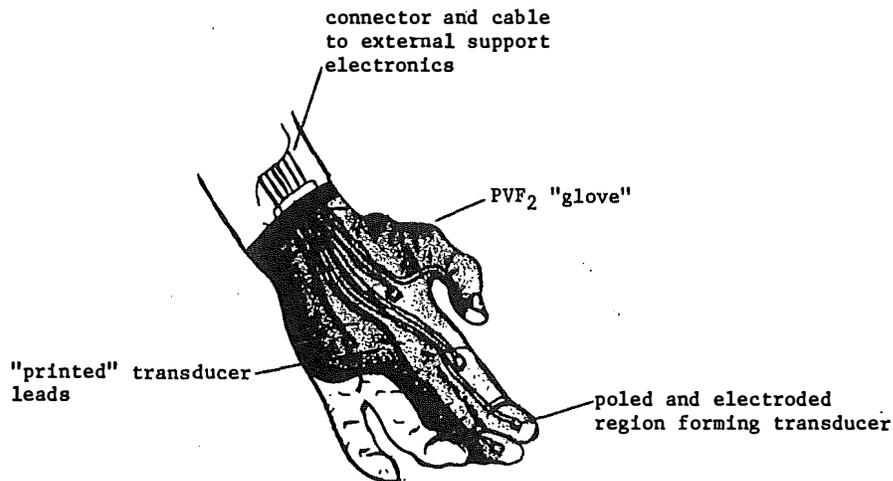


Fig. 1: Concept of force transducers incorporated into a modified glove (Courtesy of Dr. Andrew Schoenberg)

TABLE I

	<u>Force transducers</u>	<u>Position transducers</u>
Resolution	0.1 newtons (at less than 10 newtons and 1% at greater levels)	1 mm (or 0.3 degrees of angle, whichever is smaller)
Range	0.1 - 80 newtons	1-120 mm
Frequency response	d.c. to 100 Hz	d.c. to 100 Hz
Response delay	less than 2 msec	less than 2 msec

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MICROBEND FIBER OPTIC SENSOR

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ABSTRACT

Microbending induced losses in multimode optical fibers have been utilized as a transduction mechanism for an intensity modulated, fiber optic sensor. The sensor was found to be simple, very sensitive, and very stable to lead environment.

MICROBEND FIBER OPTIC SENSOR

Intensity modulation induced by microbending in multimode optical fibers has been successfully utilized as a transduction mechanism for sensing. The microbend sensor reported here is simple, very stable to lead environment, and very sensitive.

The microbend sensor is shown schematically in Fig. 1. The sensing fiber is bent along its axis periodically by a deformer, a set of two corrugated pieces. Any modulation of the amplitude of the fiber deformation introduced by an external field causes mode coupling which redistributes the light power among core modes and couples core to radiated modes. Thus, by monitoring the light power in some modes, the external field can be detected. In the simplest case, which we consider here, the power in all core modes is monitored, while the radiated modes are stripped by the absorbing coating of the fiber.

In order to optimize the sensitivity, we have studied the microbending effect in multimode fibers. One of the main results of this study is that there is a critical microbending periodicity which maximizes significantly microbending loss in fibers. Also, the microbending sensitivity was found to be proportional to λ^4 where λ is the length of the bent fiber and $0 < q \leq 1$. For fibers with optically absorbing coatings $q=1$. In this case, high sensitivity can be obtained with long lengths of bent fibers.

In order to operate as close to the shot noise limit as possible, an LED was utilized as the optical source. These sources typically have significantly lower noise levels than lasers down to very low frequencies. An added benefit results due to the absence of modal interference which otherwise would introduce strong lead sensitivity to environmental conditions.

The microbend sensor was tested as a displacement sensor using the apparatus shown in Fig. 1. The light source was a LED (for minimizing sensor noise), the leads were high NA (for reducing lead noise) commercially available fiber, and the detector was a PIN diode. The sensing fiber was a graded index fiber with an absorbing coating deformed by a pair of corrugated pieces with 14-teeth each having a 3.75 mm periodicity, which was the critical periodicity of the sensing fiber. One plate of the deformer could be displaced electrically by a piezoelectric transducer.

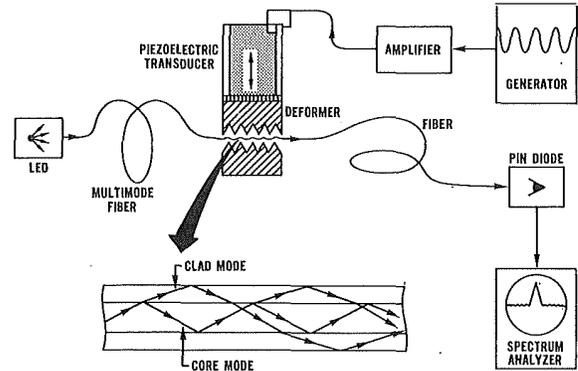


Figure 1. Experimental setup for studying the microbend displacement sensor. Insert: Displacement induced mode coupling.

Figure 2 shows a typical spectrum obtained experimentally from such a sensor with a 10Å driving displacement at 1kHz. In this case, the signal-to-noise ratio was 58dB. The minimum detectable displacement was then calculated from the signal-to-noise ratio in the frequency range of 100 to 1000 Hz and it was found to be $\sim 0.01\text{\AA}$, consistent with shot noise limited performance. The dynamic range of the sensor was found to be $> 110\text{ dB}$. Moreover, the sensor was found to be very stable with respect to the lead environment.

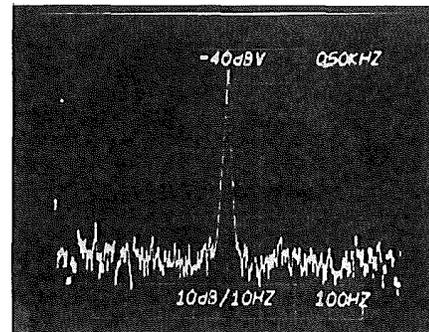


Figure 2. Spectrum obtained experimentally from the microbend displacement sensor signal at 1 kHz. Driving displacement: 10Å.

Figure 3 shows several mechanical designs for the microbend sensor for detecting various external fields. For displacement detection, only one piece of the deformer moves. As a microphone (which has been already tested successfully), the deformer is air filled and a rubber boot is used as couplant. As a hydrophone, the deformer should be liquid filled for depth compensation, and as an accelerometer, one piece of the deformer is free to move. Finally, as a magnetic sensor, the deformer is magnetostrictive.

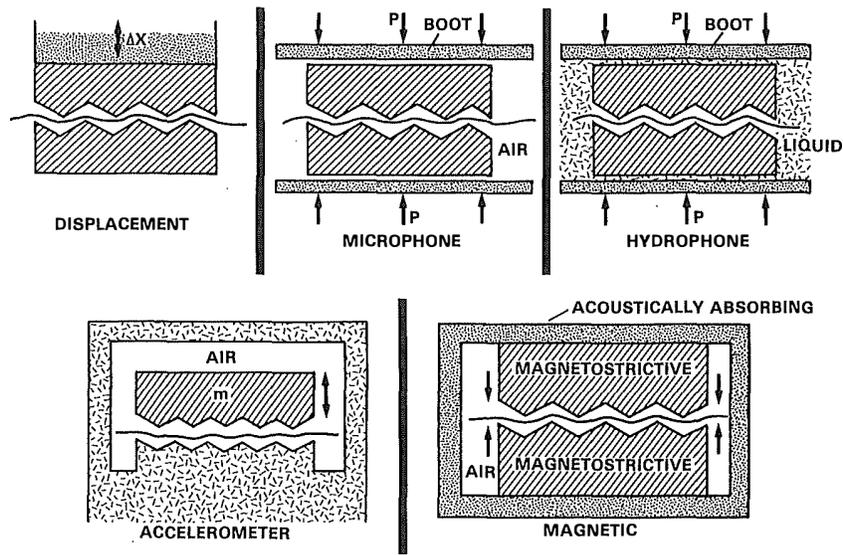


Figure 3. Microbend sensor mechanical designs for detecting various external fields.

In conclusion, we have demonstrated that the microbend sensor can be utilized to detect small displacements of the order of 0.01 . The sensor is simple, very stable to lead environment and has a wide dynamic range. Moreover, the microbend sensor can be appropriately designed for detecting various fields, such as pressure, acoustic field, acceleration, and magnetic field.

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Linear Integrated Circuits make up a large portion of the signal conditioning circuitry used to detect, amplify, demodulate, combine, compensate, linearize, digitize, and in general convert the primitive electrical output of a physical sensor or transducer into a more convenient and possibly standardized format. They are also used to provide the excitation regulation, and otherwise to control the power and stimulus applied to sensors of many kinds.

General purpose ICs such as op-amps, multipliers, and A/D converters are readily combined at board level to produce signal conditioners which are evolving toward steadily improving performance and lower costs. Collections of these functions integrated on single chips make up relatively complete signal conditioners, and the addition of the sensor to these collections seems like a desirable and very natural step.

The silicon technology used to make "Solid-State Sensors" is similar to, and in many cases identical to, silicon planar IC technology. Low cost IC manufacturing techniques are available for some of these sensors, and so the question arises: why are there so few integrated sensor/signal-conditioner chips being manufactured?

As a representative of the Linear IC design community who is keenly interested in such combinations I'd like to point out what appears to be a fundamental difficulty, in hopes of responses that will provide new vantage points from which to view and solve sensor problems. It appears to me that the same sensitivities to pressure, or chemistry, or photons, or some other phenomenon which make silicon a good transducer, makes it a bad signal conditioner. Perusal of the data sheet for a typical linear IC, used in signal conditioning, reveals that its intended function is probably pretty simple. For example, an op-amp takes little signals and makes them very large, a multiplier produces an output which is proportional to the mathematical product of two input signals, and a voltage reference provides no more than a single output voltage. The data sheet generally gives only a perfunctory explanation of the basic circuit function (since the circuit is often intended to do something trivially simple) and may devote as little as one line to specifying the desired performance.

For example in the case of the voltage reference IC it may say something like "Vref = 5.000 Volts". The remaining pages of the data sheet consist mostly of an elaborate disclaimer about unwanted sensitivities of the product and a collection of so called "Applications" which generally enumerate all the things you must do to help this little piece of silicon if you actually expect it to produce any sort of useful result.

By the time users receive the finished and tested IC it has been probe tested, sawed, diced, die mounted, wire bonded, baked, dried, evacuated and sealed: all to take any dice which have survived the fabrication process in working condition and protect them from further disturbances in the form of strain, chemical contamination, electric fields, photoelectric input, abrasion, and in short all possible influences except

the desired electrical ones. One influence that is only slightly modified by packaging is temperature and people like me like to go to great lengths to exploit the electrical properties of silicon devices while suppressing the thermal sensitivities. The data sheet then compiles long lists of how well this has all been done citing various coefficients of (in)sensitivity.

In view of all this it shouldn't be much of a surprise that silicon can be used as a sensor. It's sensitive to all manner of things in ways which are generally a nuisance but which can, on occasion, be tested in relative isolation. One of these non-surprises is that of all the possible transducer applications, temperature sensing is about the only one which has hit the big time in standard product IC form. This is the one phenomenon to which silicon circuits are sensitive and which can't be excluded by the package technology. As a result, circuit and layout designers have been forced to confront this sensitivity and understand it well in order to circumvent it in most circuits. Signal conditioning circuits can be designed to avoid expression of the inherent temperature sensitivities of silicon devices and combined monolithically with a few devices arranged to give a predictable temperature response. (1) (2).

In order to achieve similar results measuring other phenomena to which silicon devices are sensitive the co-operation of the packaging and fabrication technologists will be required. First, to devise to protect the monolithic device from unwanted exposure without excluding the measured phenomenon. And, second, to help to isolate the effect on the monolithic chip to those areas sensitized or calibrated as the sensor and away from those signal conditioning areas which would be disturbed by it.

One area where there has been some activity of this kind is in optical sensors. Something as simple as transparent lids or coatings has permitted light sensors and signal conditioning to be combined monolithically. Designs in this area include shielding the signal conditioning sections from ambient light as well as incorporating the induced photo-currents into the operation of the signal conditioning circuit. (3) (4)

Monolithic circuits combining signal conditioning with sensors for strain or chemical effects will require packaging similarly transparent to the measured quantity but opaque to other disturbances. They should also provide circuit and device designers with interesting challenges to shield portions of the chip or to design signal conditioning circuits which do not express uncalibrated sensitivities to the measured parameter.

The author will present selected topics from I.C. circuit design to illustrate the arguments presented here. And, if encouraged by questions, he will no doubt tell all (or perhaps more than) he knows of solid-state sensor design.

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A MICROMACHINED INTEGRATED SENSOR
WITH ON-CHIP SELF-TEST CAPABILITY

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ABSTRACT

A batch-fabricated multielectrode microprobe for extracellular biopotential recording in the central nervous system is described. The probe consists of thin-film conductors insulated with CVD dielectrics and supported on a micromachined silicon substrate defined using a deep boron etch-stop. Probe shank widths as narrow as 20 μ m are possible. Interface circuitry for eventual use on the probe offers per-channel amplification and multiplexing of the recorded data onto a single output lead. A 12-channel version of this circuitry dissipates 4mW from a single 5V supply and occupies an active area of 1.75mm² in 6 μ m E/D NMOS technology. Additional on-chip circuitry for on-line electrode testing is also described. This circuitry requires no additional leads and only a minimal increase in die area.

INTRODUCTION

A wide variety of integrated solid-state sensors are now being developed to extend microcomputer-based control into new areas such as health care, transportation, and automated manufacturing. These devices typically employ the full range of integrated-circuit process technology for their realization in addition to specialized processes for selectively shaping the silicon substrate (micromachining), packaging, and the deposition of special sensing materials. The use of on-chip interface circuitry with these transducing structures is now finding its way into production devices, offering the promise of reliable, bus-compatible, addressable sensors of wide applicability. In some cases, these integrated sensors offer higher reliability, higher system performance, and/or lower system cost than previous discrete or hybrid designs; however, in other cases the combination of small size with on-chip signal conditioning is allowing instrumentation not previously possible. Whatever the application, issues such as full process compatibility, the choice of an interface-circuit technology, partitioning the system electronics, selection and standardization of output signal formats, addressing modes, testability, and packaging are still largely unresolved.

This paper will comment on the above issues and illustrate them by examining one particular integrated sensor — a multichannel multiplexed intracortical microelectrode array capable of recording the activity of single neurons in the central nervous system. This probe should allow the simultaneous recording

from many neurons separated in depth through the cortex and thus allow new insights into the signal processing techniques employed by neural structures. Over the longer term, it offers the possibility of implementing closed-loop control in a variety of neural prostheses. Early forms of such microprobes [1,2] were among the first integrated sensors, and the present applications demand state-of-the-art solutions to a number of the problem areas mentioned above.

EXTRACELLULAR SINGLE-UNIT RECORDING

The use of metal microelectrodes (usually in the form of sharpened pins) has been one of the principal techniques by which physiologists, over many years, have studied the nervous system at the cellular level. Much has been learned about the operation of single neurons, but relatively little is known about their organization as functional circuits. In order to explore neural signal processing at the cellular level, simultaneous recording from many points through the circuit is certainly required; however, previous electrode technologies have not permitted the realization of multielectrode arrays small enough to avoid excessive tissue damage in use. The need to conduct such studies on a chronic basis further complicates the situation. Similar requirements hold for prosthetic applications.

Figure 1 shows a typical extracellular recording situation. When the neuron receives sufficient stimulus, its cell membrane depolarizes causing ionic currents to flow in the vicinity of the cell. In order to record the resulting voltages, the probe must be small enough to approach the cell closely with a minimum of tissue damage. Typical signal levels are a few hundred microvolts at best, with a frequency spectrum extending to perhaps 6KHz. Empirically, acceptable neural recordings require electrode impedances of 5-15M Ω at 1KHz, which for a metal electrode represents a recording area of 50-100 μ m² and a series electrode capacitance of 10-20pF.

Figure 2 shows a typical probe structure. A silicon substrate supports an array of thin-film conductors which are insulated above and below by deposited dielectric layers. Openings in the upper dielectric are used to define recording sites. On-chip electronics is needed to reduce the recording impedance levels, minimize the output leads, prevent crosstalk, and amplify the microvolt signal levels. These requirements are common to many sensing appli-

cations. Lead minimization is especially important here, and since total long-term insulation of the flexible output leads is difficult, on-chip circuitry is necessary. Circuit area must be minimized, and the total chip power dissipation should be less than 5mW to limit the temperature rise on the probe. The structure must be strong enough to penetrate the pia arachnoid over the brain and must be realizable with a process capable of high yield. In the past, the lack of such a process has prevented lithographically-defined probes from being generally available. Recent advances, particularly in the silicon micro-machining processes needed for shaping the silicon substrate, have overcome these problems.

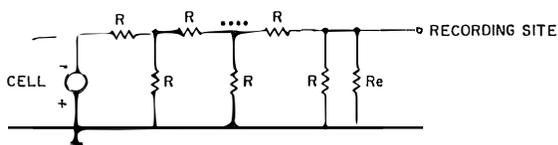
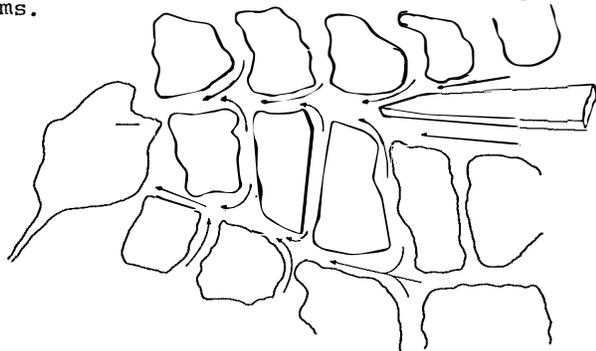


Fig. 1: Extracellular Single-Unit Recording

PROCESS COMPATIBILITY

Figure 3 shows a summary of the process for a passive probe. Fabrication begins with a p-type (100)-silicon wafer of standard thickness and doping. The wafer is first oxidized and patterned to define the intended probe areas. Next, these areas are subjected to a deep boron diffusion (1175°C for 15 hours) to define the probes. The field oxide is then stripped and a combination of thermal oxide, CVD silicon nitride, and silicon dioxide is deposited to form the lower dielectric. Conductors of tantalum or polysilicon are next deposited and patterned, followed by the deposition of the upper oxide-nitride-oxide dielectrics. These layers are patterned using a plasma process to open the recording sites and bonding areas. With the resist still in place, the exposed conductor surface is ion milled to remove any oxide, and gold is inlayed in the recording sites using ion-beam deposition. Lift-off is then used to remove the gold from everywhere except these sites and the bonding areas. The gold recording sites are thus self-aligned. The field dielectrics outside the intended probe areas are now removed using a plasma etch. Finally, the wafer is subjected to an unmasked etch in ethylene diamine-pyrocatechol-water (EDP) to separate the individual probes. This final etch dissolves the wafer and stops on the p+ probe substrate. It does not attack any of the other materials used. The completed probe chips are removed from the etch, ready for bonding.

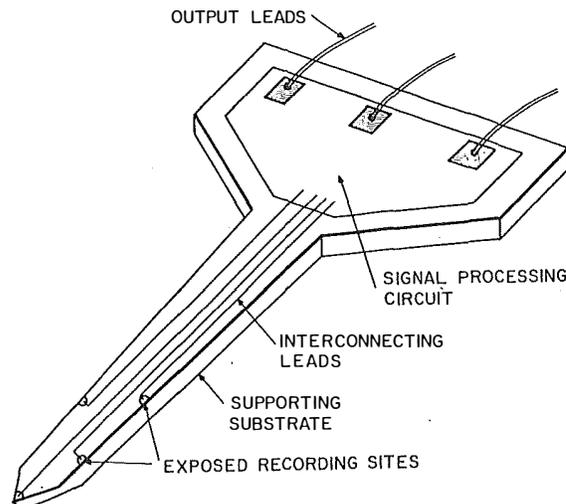


Fig. 2: A Multichannel Multiplexed Intra-Cortical Recording Array

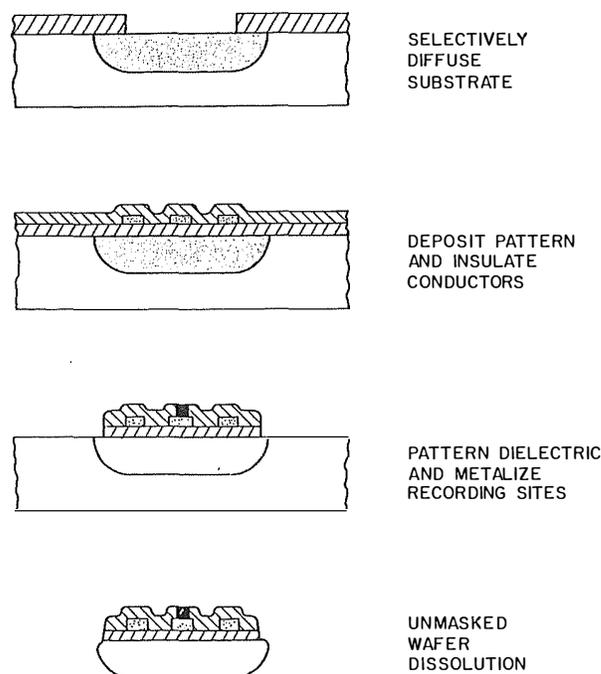


Fig. 3: Fabrication Process for a Passive Probe

This process is capable of high yields, results in very small structures, and yet requires only single-sided processing on wafers of normal thickness. All etching steps are highly selective and self-stopping. All probe features can be controlled of the order of $\pm 1\mu\text{m}$ or better. The silicon substrates can be as thick as 15-20 μm and of arbitrary two-dimensional shape. The probe edges are slightly rounded, reflecting boron outdiffusion into the field regions of the wafer. These structures are strong yet flexible and are capable of repeated insertion through pia arachnoid without damage. A minor process modification can be used to form a self-aligned support rib down the probe shank to increase its thickness without loss of dimensional con-

trol. Finally, full circuit compatibility is achieved by doping only the perimeter of the rear probe area during the deep boron diffusion, leaving the center area lightly doped for the circuitry. The passive probe process requires only four masks, two of which are shared with the circuit process when on-chip circuitry is used.

Figure 4 shows two views of a passive probe tip, while Fig. 5 shows neural activity recorded by such a structure. Figure 6 shows a probe containing active test circuitry used to establish process compatibility.

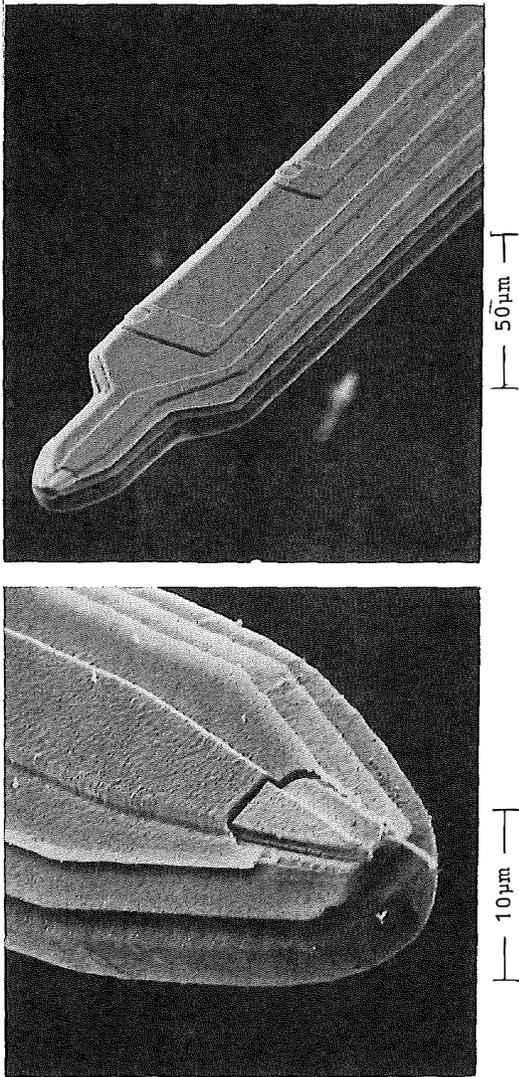


Fig. 4: Two SEM Views of the Tip Area of a Multichannel Probe

Protection of this probe structure in vivo represents a particularly significant challenge since the sensor must work in saline for extended periods and there is no room for a conventional package. Deposited dielectrics or other films must be used to ensure sensor integrity. While these packaging problems are not yet solved, some recent results are encouraging. On the probe shanks themselves, the use of CVD oxynitride films themselves may be adequate, particularly since we are primarily concerned with the ac integrity of the

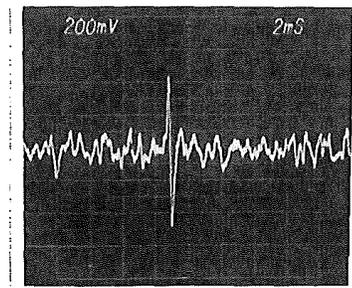


Fig. 5: Activity from Single Cortical Neurons Recorded with a Multielectrode Probe. The vertical scale is about 100µV/div.

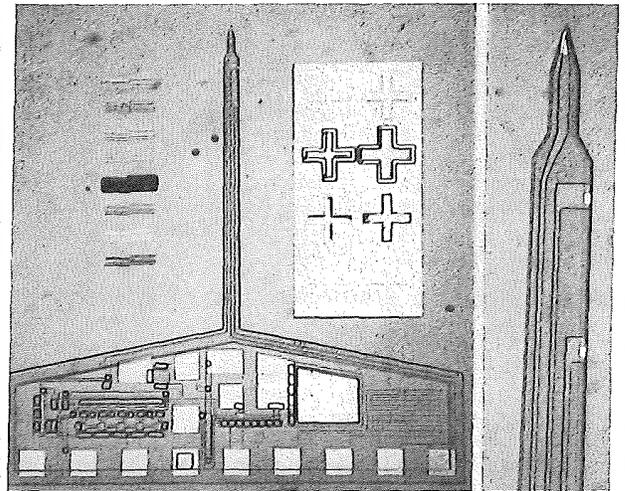


Fig. 6: A Three-Electrode Microprobe with On-Chip Test Circuitry for Studying Process Compatibility. The circuit technology is silicon-gate NMOS. An enlargement of the tip area is shown at the right.

dielectrics (100Hz - 6KHz) and the interconnect area is relatively small (0.01mm²). Over the circuitry (where appreciable DC voltages are present), as well as over the flexible output leads, thicker dielectrics can be used since they need not be photoengraved. In these areas, polymeric films appear attractive. Hughes [3] has recently reported leakage of less than 400pA/cm² for 12.5µm-thick films of Pyralin 2555 (a polyimide) after more than 250 days in saline, and the University of Missouri [4] has reported promising results with parylene. While much work remains, the packaging of sensor chips for chronic implantation is the subject of efforts in a number of laboratories, and the solutions to these problems promise considerably broader impact on the overall sensor community.

CIRCUIT DEVELOPMENT

Because of the low signal levels and high impedance associated with this sensor, on-chip circuitry is essential. While perhaps less obvious, similar situations exist for many other sensors and sensing applications. Figure 7 shows the electronics being developed for the probe. Per-channel amplifiers are

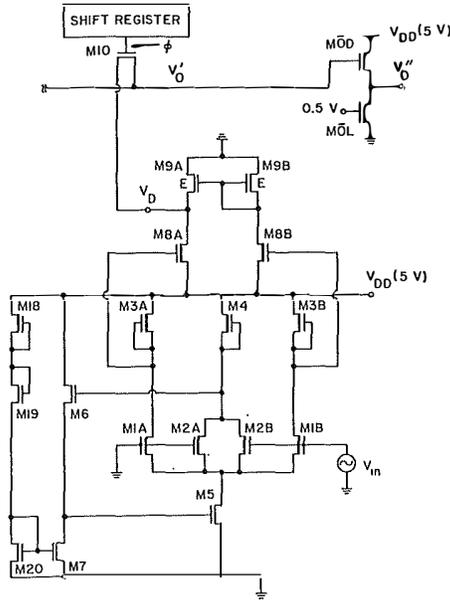
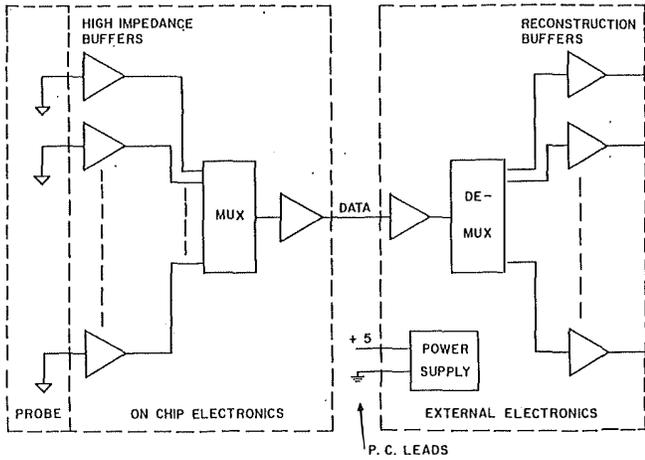


Fig. 7: Diagram of the Overall System Electronics to be used with the Multiplexed Probe and a Schematic of the On-Chip Analog Circuitry.

used for each of eleven recording electrodes. These amplifiers drive a 12:1 analog multiplexer and broadband output buffer. A total of three leads are thus required by the probe (VDD, GND, and DATA). The circuitry must operate without substrate bias. The multiplexer is driven by an on-chip two-phase dynamic shift register and a 200KHz clock to produce a per-channel bandwidth of 6KHz. A twelfth channel is used for a synchronization pulse which is decoded externally and used to regenerate the sample clock to control the demultiplexer. The external circuitry has been fully implemented and shown capable of handling 20µV neural signals with up to 40 data channels.

The on-chip circuitry to be eventually included on the probe has been implemented using a silicon-gate E/D NMOS LOCOS process as shown in Fig. 7. The input signal from the electrode is applied to one side of a differential pair of depletion-mode transistors (M1-2) capable of handling input signals near ground. This input signal is amplified and

then presented to a differential-to-single-ended converter (M8-9) before being passed to the analog multiplexer (M10) and output buffer. The allowable amplifier gain is limited to about 100 by achievable input offsets. Figure 8 shows a prototype of the full twelve-channel signal processor. The die size is 2mm x 2mm in 6µm features, including pads and a variety of peripheral and per-stage test devices and probe points. Deleting these test devices, the active die area is about 1.75mm². The measured signal gain is 20 and the total chip power dissipation is 4mW at VDD= 5V.

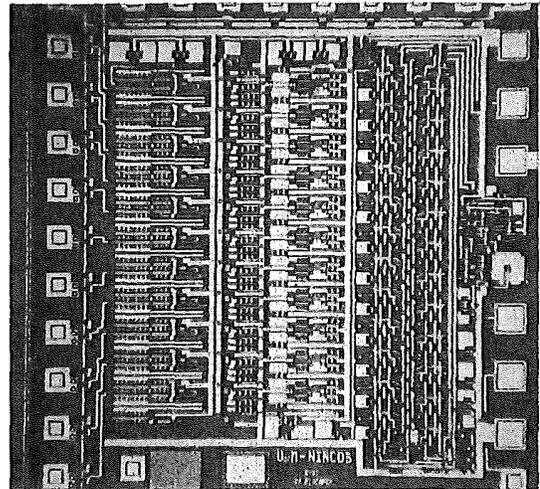


Fig. 8: A Twelve-Channel Signal Processor Prototype of the On-Chip Probe Electronics.

TESTING CONSIDERATIONS

One of the difficulties associated with the use of on-chip circuitry is that it may block the direct test access to the transducer which is available in nonintegrated system implementations. In our application here, the ability to test initially in vitro and then periodically in vivo is of major importance in evaluating device integrity in the face of long-term exposure to saline. With passive microelectrodes, the impedance magnitude is the most reliable known indicator of electrode recording ability and is the only parameter allowing electrode changes to be distinguished from physiological changes near the recording site. Thus, it is essential to preserve electrode testability in any integrated sensing structure and to do so without sacrificing normal operating performance.

Discrete electrode impedance is typically measured by injecting a known 1KHz current (e.g., 1nA) between the electrode and the recording amplifier. The resulting electrode voltage is a measure of the recording site impedance in parallel with any shunt input capacitance. Figure 9 shows the additional circuitry required to preserve testability in this integrated sensor. When the supply voltage is raised above its normal 5V level, the testing mode is enabled. The periodic strobe-channel enable signal is used as input to a four-stage counter, which produces a 1KHz clock for use in impedance testing. This clock is attenuated to a 50mV level and coup-

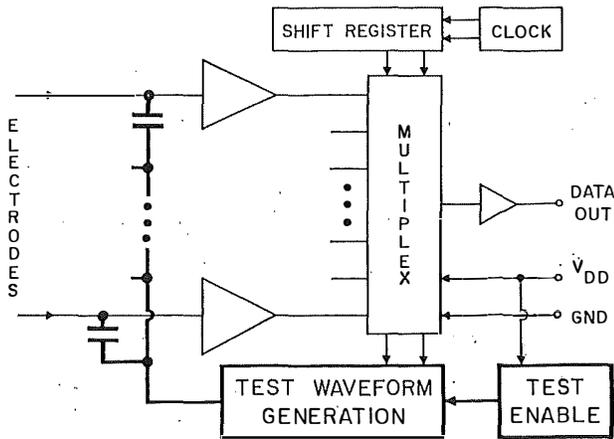


Fig. 9: Block Diagram of the On-Chip Electronics Showing the Additional Circuitry Required to Allow Self-Testing

led to the input leads using 50fF metal-to-poly crossover capacitors. The injected charge develops a signal level on the probe input lines of nominally 250 μ V, depending on the recording impedance of the particular electrode. This induced voltage is amplified and multiplexed out in the normal way.

This self-testing circuitry preserves the ability of the electrodes to be tested at any time on demand (in vitro or in vivo), requires no additional leads and only a minimal increase in die area. Being derived from the on-chip clock and passed through the normal recording channels, it also offers an additional functionality test for virtually all of the on-chip circuitry. Used in vitro with no immersion of the probe, it also offers a potential means for calibrating the gains of the individual recording channels before use.

In this particular application, great precision in the signal processing circuitry is relatively unimportant since most information is contained in the presence, general amplitude, shape, and time occurrence of each neuronal event. In many other sensing applications, great precision is required not only in the transducer but also in the signal processing circuitry [5]. In most cases, frequency- or time-multiplexed digitally-encoded output formats will be used. In these applications, as in the present one, process compatibility, circuit partitioning, high-performance analog circuit design, and packaging are central issues which are certain to occupy the sensor community for some time to come. As these issues are clarified and the problems overcome, however, entirely new application areas for integrated electronics will certainly emerge and become practical.

ACKNOWLEDGMENTS

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The electronics industry is currently experiencing a proliferation of equipment to meet the need for larger quantity, lower cost, higher speed and higher accuracy computing. The basic fuel for every one of these machines is information. Information from the physical world is first detected by sensors, which are either mechanical devices or humans. This information must then be transported and fed into the computer as digital information. The process is done by humans again, or by electronic equipment. At this point, the computer can process this raw information along with other parameters and provide a logically deduced output using its software algorithms. Advances in computer hardware and software algorithms must be matched by comparable advances in sensor and data acquisition areas in order to provide the computers with the information fuel that they require. Silicon technology provides the means for achieving these needed advances in sensing and data acquisition.

Sensor Inputs

Sensors that are used with digital systems typically convert such physical information as pressure, temperature, optical characters or sound into various electrical signals. These signals are often represented as changes in voltages, currents, impedances or frequencies, which must subsequently be changed into a digital word that can be used by a computer. In addition, this digital word needs to find its way to the correct computer port at the correct time, and eventually route its way to a memory location so that it can be used as a piece of information upon which the computer can act.

The Need for Information

A unifying feature of the many potential applications of digital information systems is the need for accurate, rapid, and unexpensive information. Traditional techniques of human data entry fall short in each of these characteristics. Major needs for automatic data acquisition can be seen by looking at examples of current applications. In classical process control and industrial monitoring, as well as factory automation and robotics, there is a definite need for accurate information on multiple parameters. Computers and controllers are being used to respond to routine changes, but human monitoring is still used extensively to detect additional information and override the computer control. In aerospace applications, the speed and accuracy of a computer response is needed to overcome human limits, yet the human override still exists.

Similarly, commercial applications such as bar-code accounting systems, weighing systems and security systems currently use sensors and data acquisition. Lower cost accurate sensors that are more easily installed and interfaced with computers would undoubtedly be used for more complete information to the computer. With the exception of such simple systems as those presently found in automobiles and security systems, consumer applications of information processing systems are also limited to uses that rely on human generated information.

Information Processing Hardware

Advances in computer technology have intensified the need for comparable developments in sensors, actuators and software. Powerful low-cost portable machines permit wholesale digital signal processing in distributed locations, and large high-speed mainframe computers give the capacity to perform large volumes of logic operations. A result of all of this capacity is that the cost per logic operation has been lowered and the capacity of the computing base has increased. This is further evidence of the need for a matching increase in quality of input output devices. The limiting cost of a control system is rapidly approaching that of the sensors and actuators which interface the real world to the computer.

Sensor Performance

Important performance parameters for sensors include accuracy, speed, linearity and compensation for parasitics. Cost, size and materials compatibility are also significant factors. Sensor structures micromachined in silicon have many significant advantages over traditional materials in these areas, primarily from the ability to batch fabricate precision structures in silicon and the strength and inert characteristics of the material. Coupled with signal processing on the same chip, accuracy and compensation can be achieved to meet the needs for widespread application in digital systems.

Data Acquisition

Silicon circuitry also provides the means to process the signals from the physical sensor structure and format it for use by the computer. In addition, it can be addressed by the computer so that the correct information is received at the desired port at the required time. Data acquisition equipment to date ranges from devices using such standard serial communication formats as RS232C through higher speed parallel devices. Single input devices through recent multisensor networks have used a diverse set of architectures. In addition, there are a number of special purpose interface formats such as frequency encoding or special handshake and addressing formats to reduce processor and acquisition overhead.

Algorithms

To use sensory information effectively, the computer needs to interpret it and relate it in a logical manner. Approaches such as distributed processing, compensation, and methods for relating information must be developed along with sensor, acquisition and computer hardware.

Realizing Information Systems

The computer industry has taken an early lead in developing tremendous computing and information processing hardware. Software and algorithms for handling information are also under development which are essential ingredients for an effective information processing system. Recent developments in micromachined silicon sensor structures and data acquisition systems promise comparable breakthroughs in fabricating these components.

SOLID STATE SENSOR RESEARCH AT HONEYWELL:
ACTIVE THIN FILMS PLUS MICROSTRUCTURES

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The development of Si-based solid state sensors has proceeded over the last decade and a half at Honeywell. Many such sensors, based on several technologies, are in production at Micro Switch and the Solid State Electronics Divisions. The first of these sensors utilized physical phenomena in the silicon itself to sense the desired quantities: The Hall effect for sensing magnetic fields, optical carrier generation for light sensing, and the piezoresistance effect for strain sensing. A vast number of Hall chips have been produced for keyboards, automobile distributors, and other high-volume applications. Auto-focus chips using arrays of photodiodes and sophisticated signal processing are used in many types of cameras. A large family of silicon piezoresistive pressure sensors is produced. These types of sensors are easily and inherently "integrated," since they are actual silicon devices.

Since the range of phenomena useful for sensing in silicon is limited, more recent developments have utilized thin films added to the silicon, active films in which useful interactions take place. Examples include thin film metals with high TCR for resistive temperature sensors, and thin films of magnetic alloys for sensing magnetic fields through the magnetoresistance effect. These devices utilize silicon only as a convenient substrate with well-developed processing technology. Integration with active IC electronics is generally possible, but requires development of compatible processes. The decision to integrate or not is usually based on business and economic arguments. Such devices are described in a talk elsewhere in this conference.

The most advanced solid state sensor research at Honeywell involves combinations of active thin films with silicon microstructure technology. The thin films utilized include zinc oxide (ZnO) piezoelectric films, useful for strain sensing or for generating acoustic waves. Microstructure technology includes use of simple silicon diaphragm structures etched from the back side of the wafer, and more complex structures formed by etching from the front side. Devices being studied include acoustic and seismic sensors, and an air flow sensor.

These devices will now be described in more detail.

The acoustic and seismic sensors are similar devices using a piezoelectric film of ZnO as a strain sensor on the top of an etched silicon diaphragm. A unique annular electrode design is used to cancel signals due to the pyroelectric effect in ZnO; it also allows all connections to be made in the ZnO/Si interface plane, avoiding step coverage problems, and increases the sensitivity by a factor of two over a simple circular electrode design. Typical devices use diaphragms 3mm in diameter and 30 microns thick, with ZnO films of 1 to 3 microns. When packaged so as to expose one side of the diaphragm to an acoustic signal, sensitivities of 25 microvolts per microbar were obtained, with a signal to noise ratio of 5:1 at 2 microbars. The response was flat to within 3 to 5 dB over the measured frequency range from 10 Hz to 10 kHz, and a low frequency cutoff of 0.1 Hz was obtained. The excellent low frequency response is a unique feature of this sensor. Some of these devices have been integrated with simple MOS electronics. Integration is particularly desirable for this sensor, since high sensitivity requires direct, low-capacitance connection of the ZnO structure to a high input impedance amplifier.

The same basic device can be used as a seismic or vibration sensor by attaching a proof mass to the diaphragm. Under acceleration along the axis perpendicular to the chip plane, the proof mass deflects the diaphragm. This strain creates a piezoelectric charge in the ZnO which is detected by a high-impedance amplifier. The mass can be as simple as a lead ball glued onto the diaphragm, or can be a more complex etched structure. Analysis predicts sensitivities of about 25 millivolts per G for proof mass of 30 mg. Several of these seismic sensors have been fabricated and are currently being tested.

A sensitive, miniature gas flow sensor has been demonstrated, using a combination of thin film resistive elements and an etched microstructure. Its operation is much like a miniature hot wire anemometer: A central thin film resistive heater element is flanked

by a pair of resistive thin film temperature sensors. The heater and temperature sensors are part of a microstructure formed by etching, and are thereby thermally isolated from the silicon chip. The difference in temperature between the two sensors is measured. In the absence of flow their temperatures are the same. With flow along the structure, the upstream sensor is cooled and the downstream one heated, resulting in an output signal. The sensor has high sensitivity to flow and low power requirements because of its small size and the thermal isolation provided by the microstructure. Air flow response from a few feet per minute up to thousands of feet per minute has been obtained. Differential pressure response well below 1 inch of water column (249 Pa) is obtained in air. The response is bidirectional, indicating flow direction as well as velocity.

The total response is dependent on the sensor chip characteristics, control of the air flow, and the electronic mode of operation of the device. Performance such as this in a low cost, low power Si chip device capable of measuring low gas flows and even differential pressures leads to many exciting application possibilities which cannot be addressed by existing sensors.

The new sensors described here are only the beginning of what can be developed with the combination of thin films and silicon microstructures. Complete integration with electronics may be more difficult because of the cascading of process sequences for fabricating electronics, active thin films, and microstructures. The payoff is in the creation of sensors which have unique capabilities unavailable in conventional devices.

NEW DIMENSIONS FOR INTEGRATED SENSORS

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Integrated Sensor is a designation that invites comparison with the term Integrated Circuit. As is the case with ICs, integrated sensors should be considered as new components that open wholly new dimensions for system design.

Integrated sensors became a reality in the 1960s with the exploitation of the sensitivities of silicon to radiation (electromagnetic as well as nuclear), and to inputs such as temperature, magnetic field, and stress. A considerable maturity has been reached in design for these inputs.

Silicon Hall-effect sensors are well developed and accurate, but they are generally rather large devices which operate well in magnetic fields greater than 100 gauss. Magnetic detectors with sensitivities below one gauss can be attained with carrier-domain magnetometers (CDMs). In integrated sensors these elements can be incorporated with components such as current mirrors, differential comparators, or Schmitt triggers to provide new modes for detection and signal processing. The magnetic signal can be represented as a differential current, a differential voltage, or as a modulated frequency. Because of their high sensitivity CDMs are responsive to the magnetic fields of relatively small currents, and can therefore be calibrated by "on-chip" circuitry.

Despite compatibility problems with conventional IC processing, anisotropic etching of silicon has been employed frequently for micromechanics, an important technology for integrated sensors. Anisotropic etchants are, however, not necessary to make free-standing polycrystalline silicon structures which can be formed by removing the supporting oxide layers with standard HF etching [2]. Doubly supported beams formed of polysilicon have been incorporated into a vapor sensor that detects a small loading change when xylene is absorbed by a polymeric coating on a polycrystalline silicon beam. A complete discussion of this sensor will be given elsewhere, but research on it has given indication of the durability of polysilicon as a material for micromechanics. In the vibrating beam, there is no change in properties after more than 10^{10} flexures [3]. Young's modulus for polycrystalline silicon has been obtained through experiments with this micromechanical structure, and the stress at the interface between polycrystalline silicon and silicon dioxide has been studied [4].

Piezoelectricity in thin films deposited on silicon ICs provides an alternative to piezoresistance in silicon for stress sensing. Sputtered ZnO films have been shown to be suitable for this purpose, and have been combined with micromechanics to produce a high-performance accelerometer [5]. Sputtered ZnO has also been used as a pyroelectric with applications to mass air-flow sensing [6].

Finally, silicon technology combined with sputtered ZnO films also makes possible surface-acoustic-wave integrated sensors for vapor detection. These systems have potentially great sensitivity and flexibility. Especially significant for integrated-sensor design is the finding that acoustic energy can be transferred through plate modes in thinned silicon diaphragms. This provides a means to keep the electronics of the sensing system remote from the interaction surface [7].

Clearly, old and accepted units will be used to measure the integrated-sensor systems that are built by exploiting these new dimensions. The units are simple: success or failure. The odds -- and the state of maturity of today's electronics -- strongly favor success.

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COMPENSATION AND CALIBRATION OF A MONOLITHIC FOUR TERMINAL
SILICON PRESSURE TRANSDUCER

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A monolithic silicon pressure transducer has been developed which employs a single four terminal shear stress sensitive piezoresistive strain gauge in place of the more common Wheatstone bridge construction. The gauge, which is called a transverse voltage strain gauge, was placed at the midpoint of the edge of a square diaphragm at an incline angle of 45° in order to maximize sensitivity and minimize non-linear effects. Silicon pressure transducers fabricated using this strain gauge technology yield sensitivities of 200-300 $\mu\text{V}/\text{V}/\text{kPa}$ for a 100 kPa full scale pressure range with non-linearity and pressure hysteresis errors of less than $\pm 0.1\%$ FS. The variation in zero pressure offset is typically on the order of $\pm 8\%$ FS with a temperature coefficient of offset of $\pm 0.025\%$ FS/°C relative to the 25°C value. The temperature coefficient of full scale span is $- 0.19 \pm 0.02\%$ /°C while the temperature coefficient of the input impedance is $0.24 + 0.02\%$ /°C.

In order to improve the performance of the transverse voltage strain gauge pressure transducer over temperature a method was developed by which a compensation and calibration circuit is fabricated on the same substrate as the strain gauge using deposited thin film resistive material. The resistances can subsequently be adjusted to the required values for each transducer using high speed, computer controlled laser trimming techniques. This design has yielded calibrated transducers with total errors, including non-linearity, hysteresis, thermal offset shift and thermal span shift, of less than 1% from 0°C to 85°C.

It is the goal of this contribution to describe the salient features of the design of the transverse voltage pressure transducer along with package design and assembly considerations that help preserve the performance of this device. In addition, a description of the compensation and calibration circuit including important processing and laser trimming techniques will be given.

INTRODUCTION

Monolithic silicon pressure transducers offer many desirable features, being small in size, low in cost, and having good performance characteristics such as high sensitivity, small non-linearity and pressure hysteresis errors, and excellent immunity to mechanical shock and vibration. They are manufactured using the mass production, batch processing technology of the semiconductor industry, allowing hundreds of devices to be fabricated simultaneously on a single silicon substrate. A cross-sectional view of a typical silicon pressure transducer device is shown in Fig. 1.

The most common design for silicon pressure transducers is to arrange four stress sensitive resistors in the form of a Wheatstone bridge [1-3]. When pressure is applied to the diaphragm containing these resistors, the resulting stresses cause the resistors to change in value, unbalancing the bridge and generating an output

voltage proportional to the applied pressure. While very high performance pressure transducers can be made using the Wheatstone bridge construction, the calibration and temperature compensation of these devices is often complex due to part-to-part variations in the characteristics of these devices. These part-to-part variations are to some degree inherent in the design of silicon pressure transducers employing the Wheatstone bridge construction. Kim and Wise [4] have published a detailed analysis of the problems associated with the temperature sensitivity variations of a bridge design. In particular, the close matching of the characteristics of the resistors in the bridge required to obtain a well behaved device is difficult to achieve using even the most advanced state-of-the-art semiconductor processing technologies. Therefore, it was concluded that if the full cost advantage of the silicon pressure transducer technology was to be realized, a design was needed which eliminated the need for closely matched stress sensitive resistors. In order to achieve this objective, it was necessary to review the theory of piezoresistivity in semiconductors and the manner in which this theory determines the design of silicon pressure transducers. The result of this study was the transverse voltage strain gauge design, a four terminal piezoresistive device which gives an output voltage proportional to the applied pressure from a single diffused stress sensitive silicon resistor.

THEORY OF TRANSVERSE VOLTAGE STRAIN GAUGE DESIGN

The piezoresistive effect in semiconductors can be described in terms of a phenomenological theory which relates changes in the electrical conductivity of the material to the applied stress through an empirically determined set of constants called the piezoresistive coefficients. In a cubic material such as silicon, the phenomenological theory of piezoresistivity can be expressed by an equation of the form [5]

$$E_i/\rho_o = I_i + \sum_{jkl} \pi_{ijkl} I_j T_{kl} \quad (1)$$

where ρ_o is the unstressed bulk electrical resistivity of the material, E_i and I_i are the electrical field strength and current density respectively parallel to the x_i crystallographic axis, T_{kl} is the stress acting on the plane perpendicular to the x_i axis in the x_k direction and π_{ijkl} is the piezoresistive coefficient. These piezoresistive coefficients are analogous to the elastic constants in the manner in which they transform from one coordinate system to another and in their relationship to the symmetry of the crystallographic structure of the material [6].

This expression can be further simplified by adopting the Voigt notation for the stress tensor, where a 3x3 rank two tensor T_{kl} is replaced by a 1x6 rank one tensor t_k , and applying the conditions of cubic symmetry to the resulting 6x6 rank two piezoresistive coefficient tensor π_{jk} . Under these conditions, the expression given in eqn. (1) reduces to the following three equations [5]:

$$E_1/\rho_o = I_1 [1 + \pi_{11}T_1 + \pi_{12}(T_2 + T_3)] + \pi_{44} (I_2T_6 + I_3T_5) \quad (2)$$

$$E_2/\rho_o = I_2 [1 + \pi_{11}T_2 + \pi_{12}(T_1 + T_3)] + \pi_{44} (I_1T_6 + I_3T_4) \quad (3)$$

$$E_3/\rho_o = I_3 [1 + \pi_{11}T_3 + \pi_{12}(T_1 + T_2)] + \pi_{44} (I_1T_5 + I_2T_4) \quad (4)$$

These results are expressed in terms of the three independent piezoresistive coefficients π_{11} , π_{12} , and π_{44} as required by the conditions of cubic symmetry.

In the case of a silicon pressure transducer, the stress sensitive resistor can be assumed to be subjected to a state of plane stress due to the plate like nature of the thin diaphragm structure. If it is assumed that the current axis of the resistor is parallel to the x_1 crystallographic axis and the resistor lies in the plane normal to the x_2 crystallographic axis, this plane stress can be described in terms of the two uniaxial stress components, T_1 and T_2 , which act respectively parallel and perpendicular to the current axis of the resistor, and the shear stress component, T_6 , which acts in the plane of the resistor. All other current and stress components are equal to zero in this case. For this special case of a single stress sensitive resistor subject to a plane stress, there are only two non-zero field equations:

$$E_1/\rho_o = I_1 (1 + \pi_{11}T_1 + \pi_{12}T_2) \quad (5)$$

$$E_2/\rho_o = \pi_{44} I_1 T_6 \quad (6)$$

The effect described by eqn. (5) is that normally employed in silicon pressure transducers of the Wheatstone bridge construction. It manifests itself as an apparent change in the resistance of the stress sensitive resistors in the bridge. By the judicious placement of these resistors with respect to the stress field in the silicon diaphragm and their orientation relative to the crystallographic axes of the material, it is possible to obtain stress sensitive resistors which either increase or decrease in resistance when pressure is applied to the diaphragm. Under these conditions, the Wheatstone bridge becomes unbalanced when pressure is applied and the output signal of the bridge can be maximized.

The second effect described in eqn (6) is generally ignored in the design of silicon pressure transducers. It is a consequence of the loss of the block diagonal property of the resistivity tensor as a result of the piezoresistive effect which causes non-zero off-diagonal components to appear in this tensor property when the material is stressed. It is manifested as an electric field which develops perpendicular to the current axis of the resistor. The significance of this result is that this electric field can be measured in a single stress sensitive resistor. This is the theoretical basis for the design of the transverse voltage piezoresistive strain gauge. A four terminal gauge was proposed by Pfann and Thurston [6] to measure biaxial stress while Mallon et al [7] have described a similar type of strain gauge for measuring pressure.

DESIGN OF TRANSVERSE VOLTAGE PRESSURE TRANSDUCERS

The design of silicon pressure transducers is governed primarily by two considerations: (1) the sensitivity of the piezoresistive strain gauge to

stress and (2) the distribution of the pressure induced stresses in the diaphragm structure. These two factors directly effect the magnitude of the output of the pressure transducer and the linearity of this output with respect to the applied pressure. This is true in the design of silicon pressure transducers employing the transverse voltage strain gauge technology as well as those of the Wheatstone bridge construction. One of the most significant properties of the piezoresistive effect on semiconductors is the dependence of this effect on the crystallographic orientation of the stress sensitive resistor. This is a consequence of the tensorial nature of this phenomenon and the manner in which this tensor property transforms from one coordinate system to another. As noted previously, this property can be employed to optimize the sensitivity of the silicon pressure transducer.

In the case of the results presented in eqns. (5) and (6) it was assumed that the current axis of the stress sensitive resistor was parallel to a crystallographic axis and that this resistor was located in a plane perpendicular to a crystallographic axis, a highly specialized case. However, similar expressions can be derived for any general case [6]. In the design of silicon pressure transducers it is not necessary to consider all arbitrary orientations since there are other factors which also influence the choice of the crystallographic orientation. Primary among these is the manner in which the silicon diaphragm is fabricated.

For silicon pressure transducers to be fabricated using the batch processing technology of the semiconductor industry, chemical etching is the preferred process for the fabrication of the diaphragm structure. However, since this diaphragm is generally very thin compared to the thickness of the silicon substrate material, a considerable etch time is required to form the diaphragm. Therefore, it is desirable to use an etching process which is highly anisotropic in order to minimize the lateral spreading of the dimensions of the diaphragm during the etch process. Anisotropy is also important if it is desired to fabricate a diaphragm of uniform thickness such as is shown in Fig. 1. Almost without exception solutions which etch silicon anisotropically tend to etch in the (001) directions most rapidly and in the (111) directions most slowly [8]. Therefore, a substrate orientation normal to a (001) direction is typically chosen for such transducers. Under this condition, etchants such as KOH will produce either square or rectangular diaphragm structures which lie in the (001) crystallographic plane with the underlying cavity bounded by (111) type crystallographic planes. For this reason (001) silicon substrates were chosen for the design of the transverse voltage strain gauge pressure transducer.

In the special case of a (001) oriented silicon substrate, it can be shown [6] that the results derived in eqns (5) and (6) are valid for any arbitrary orientation of the current axis in this plane if the crystallographic piezoresistive coefficients π_{11} , π_{12} , and π_{44} are replaced by the corresponding coefficients transformed into the coordinate system defined by the current axis, the normal to the plane of the substrate, and the cross product of these two vectors. Using these transformed piezoresistive coefficients, the two electric field equations become

$$E_1'/\rho_o = I_1' (1 + \pi_{11}' T_1' + \pi_{12}' T_2') \quad (7)$$

$$E_2'/\rho_o = \pi_{44}' I_1' T_6' \quad (8)$$

where the prime superscript indicates that all the quantities are referred to the transformed coordinate

system. Because of their orientation parallel and perpendicular to the current axis respectively, the stress components T_1' and T_2' are frequently referred to as the longitudinal and transverse stress components. Their associated piezoresistive coefficients, π_{11}' and π_{12}' are denoted as the longitudinal and transverse piezoresistive coefficients respectively. The coefficient π_{44}' associated with the shear stress component T_6' is similarly referred to as the shear piezoresistive coefficient.

Figure 2 shows how the piezoresistive coefficients π_{11}' , π_{12}' , and π_{44}' vary with the orientation of the current axis relative to the (110) flat on a (001) silicon substrate. These values were computed for a p-type silicon resistor using the experimentally determined values of Smith [9]. Note that for resistors parallel and perpendicular to the wafer flat, π_{11}' and π_{12}' are at their extreme values while the shear coefficient π_{44}' is maximized at 45° to the wafer flat.

For silicon pressure transducers employing the Wheatstone bridge construction it is common for the stress sensitive resistors to be oriented parallel and perpendicular to the (110) wafer flat on (001) substrates since, as can be seen from eqn. (7), these orientations maximize the sensitivity of the resistors to the uniaxial stresses T_1' and T_2' . In contrast, for devices employing the transverse voltage strain gauge design, the optimal orientation is at 45° to the wafer flat since this maximizes the shear piezoresistive coefficient π_{44}' and hence, from eqn. (8) the voltage perpendicular to the current axis of the resistor.

For both the Wheatstone bridge construction and the transverse voltage strain gauge design, the stress state within the silicon diaphragm is determined by the geometry of the diaphragm structure and the elastic properties of the substrate material. A wide variety of geometries are employed, ranging from circular to rectangular to square diaphragms. In most silicon pressure transducers the placement of the stress sensitive resistors on this diaphragm structure is such that the resistors are subject to a stress state which maximizes the piezoresistive effect. In some cases, however, it is necessary to compromise this consideration in order to achieve good linearity. A primary factor which influences the linearity of the output voltage of silicon pressure transducers is the linearity of the pressure versus stress relationship in the diaphragm structure when integrated over the active area of the stress sensitive resistors. For this reason, the resistors are often oriented such that they lie along lines of constant stress in the diaphragm structure. It is often necessary to greatly extend the dimensions of the diaphragm in order to achieve such a condition over the entire active area of the stress sensitive resistors. In the case of the design of the transverse voltage strain gauge pressure transducer, the condition of constant stress was not felt to be a major consideration, since the active area of this type of strain gauge is quite small, being confined to the region common to the four terminals of the device. In the final design for this device the active area of the transverse voltage strain gauge is less than $1 \times 10^{-3} \text{ mm}^2$ which, in comparison to the total diaphragm area of over 2 mm^2 , is virtually a point condition.

To determine the optimal location of the transverse voltage strain gauge, a finite element stress analysis model was employed to calculate the stress distribution in the diaphragm structure. While a wide variety of diaphragm geometries were evaluated, a square diaphragm was desired in order to minimize the total die size of the device. Figure 3 shows the results of a finite element analysis for a square dia-

phragm which is rigidly clamped at its boundaries. These results are shown in terms of the principal stress distribution at the centroid of the finite elements. These stresses are indicated in Fig. 3 by orthogonal vector pairs where the length of the vectors pairs where the length of the vectors correspond to the magnitude of the principal stresses and their orientation corresponds to the orientation of the principal stress coordinate system. Only one eighth of the total diaphragm area is shown in this figure, since the remainder of the total stress distribution can be generated by reflection across the symmetry planes of the square diaphragm.

As can be seen in Fig. 3, the region of maximum stress is located at the edge of the diaphragm on the centerline of the square diaphragm. At this point, the principal stress coordinate system is coincident with the coordinate system defined by the edges of the diaphragm, with the principal stresses being parallel and perpendicular to the edge of the diaphragm. The slight deviation from this condition shown in Fig. 3 is due to the fact that the centroid of the finite element is not located exactly at the center of the edge of the diaphragm. By definition the principal stress coordinate system is oriented such that the shear stress component is zero. It is well known, however, that the maximum shear stress state exists in a coordinate system rotated by 45° with respect to the principal stress coordinate system. Therefore, from the results in Fig. 3 and the shear stress dependence given in eqn. (8), the optimum location for the transverse voltage strain gauge on a square clamped diaphragm is near the center of the edge of the diaphragm oriented at 45° to this edge. Under these conditions, the transverse voltage strain gauge is oriented such that the coordinate system defined by the current axis, the substrate normal, and the cross product of these two vectors corresponds to the state of maximum shear stress in the diaphragm structure.

Recalling that the shear stress piezoresistive coefficient, π_{44}' is maximized when the current axis of the transverse voltage strain gauge is oriented at 45° to the (110) wafer flat on a (001) substrate, it can be seen from eqn. (8) that, if the edge of the diaphragm is also oriented parallel to the wafer flat, the output of the pressure transducer will be maximized. Fortunately, such a condition can be easily satisfied in silicon pressure transducers, since the normal orientation of an anisotropically etched diaphragm on a (001) substrate is such that the edges of the diaphragm are parallel and perpendicular to the (110) wafer flat as a result of the crystallography of the substrate.

Figure 4 shows schematically the layout of a silicon pressure transducer employing a transverse voltage strain gauge using the design rules developed in this section. As can be seen in this figure, the stress sensitive resistor is oriented at 45° to the edge of the square diaphragm and is located along the center line of the diaphragm near the edge. The two voltage taps used to sense the transverse field generated by the pressure induced shear stress are located at the midpoint of the resistor at right angles to the current axis. These voltage sense taps can be fabricated with the same photolithography and diffusion steps used to fabricate the stress sensitive resistor itself; allowing these taps to be very accurately positioned with respect to the resistor. The importance of this ability will be discussed later. A secondary, heavily doped enhancement diffusion is employed to minimize the total impedance of the device, to eliminate the need for metal runs on the silicon diaphragm, and to provide for good ohmic contact to the metallization.

Since silicon pressure transducers are very sensitive strain gauges, special requirements are placed on the packaging schemes used to manufacture the devices. In order to maintain the best possible performance of the transverse voltage strain gauge pressure transducer as well as take full advantage of the mass production techniques of the semiconductor industry, a package was designed that reduces non-pressure related stresses to a minimum as well as provide a form that lends itself to high speed automated assembly and testing techniques. A cross-sectional view of this package is shown in Fig. 5. After processing is complete the transverse voltage pressure transducer wafer is bonded to a silicon substrate using a glass frit that has a thermal coefficient of expansion close to silicon (see Fig. 1). The bonded pair of wafers are sawn and the individual die bonded to the base plate using a soft silastic adhesive which isolates the transducer die from assembly and thermally induced stresses. After attaching wires to the die the package is filled completely with a soft, hydrostatic methyl-silicone gel to protect the surface of the die from harsh environments and a metal cap heat staked to the top. The chip carrier concept is similar in assembly to lead frame type assembly that is prevalent in the semiconductor industry. The package was designed with chamfered surfaces in order to provide an area where a pressure tight seal can be made quickly and reliably using an automated clam-shell type of test fixture. The package is symmetrical around the plane of the leads, thus enabling the pressure signal to be applied from either side when used in a differential or gauge application as well as radially distributing any stresses due to mounting so that these stresses will not reach the transducer die.

COMPENSATION AND CALIBRATION OF THE TRANSVERSE VOLTAGE STRAIN GAUGE PRESSURE TRANSDUCER

The performance characteristics described in this section are based on the results of the testing of production quantities of the MOTOROLA "X-ducer" MPX series of monolithic silicon pressure transducers which employ the transverse voltage strain gauge technology [10]. All characteristics are given for a 3.00 Vdc supply voltage and at 25°C unless otherwise noted. Both full scale span and zero pressure offset values are ratiometric with the supply voltage.

A typical output voltage versus applied pressure curve for the MOTOROLA MPX-100D silicon pressure transducer is shown in Fig. 6. This is an uncompensated, uncalibrated differential pressure transducer covering the pressure range from 0 to 100 kiloPascals (kPa) measured without any externally applied calibration or temperature compensation techniques. The full scale span of this device is typically 60 mV with a nominal temperature coefficient of full scale span of $-0.19\%/^{\circ}\text{C}$ over the temperature range of -40°C to $+125^{\circ}\text{C}$. Since the offset of this type of transducer depends not on matching resistors but on how well the transverse voltage sense taps are aligned, and this is accomplished in a single photolithography step, the offset was designed purposely to be positive in sign in order to simplify the design of compensation and calibration circuits using this device. The offset typically ranges between 15mV and 25mV with a nominal temperature coefficient of $\pm 15\text{ uV}/^{\circ}\text{C}$. The temperature coefficient of offset is relatively small due to the fact that again the need to match resistors and TCRs

is eliminated in this design and the only change in offset over temperature is due to package related stresses. The resistance of the transducer is typically 460 ohms with a nominal temperature coefficient of resistance of $0.24\%/^{\circ}\text{C}$. Both the non-linearity and the pressure hysteresis errors are typically on the order of $\pm 0.05\%$ FS. The non-linearity error is measured relative to the end-point straight line fit to the output values at the extreme points of the operating pressure range.

While this device is not temperature compensated and there is part-to-part variability in sensitivity and offset, it was designed such that it can be easily calibrated and temperature compensated over a fairly extensive temperature range using passive components. To see how this is accomplished let us consider the results given in eqn. (8) expressed in terms of the supply voltage, V_o , and the differential output voltage ΔV . For a resistor of length l and width w , the relationship between the output voltage and the supply voltage can be shown from eqn. (8) to be given by

$$\Delta V = (w/l)\pi^{1/4} T_{44}^{1/6} V_o \quad (9)$$

As can be seen from this relationship the output voltage of the device is ratiometric with the supply voltage. Thus, both the offset and full scale span can be calibrated by adjusting the supply voltage and shunting currents in the output taps. The decrease in the output voltage with increasing temperature is due to the temperature dependence of the piezoresistive coefficient $\pi_{44}^{1/6}$. This dependence is shown in Fig. 6. It is important to note that the results shown in the figure are for a constant supply voltage. Therefore, if the supply voltage were increased with temperature in the proper manner, it would be possible to keep the output voltage constant due to the ratiometric behavior of this device. It is possible to accomplish this by placing a resistor in series with the transducer and driving the circuit at a constant voltage. Since the TCR of the transducer is $+2400\text{ ppm}$ the supply voltage across the transducer will increase at the rate of $+2400\text{ ppm}$ and will overcompensate the decrease in full scale span of -1900 ppm . However, the "effective" temperature coefficient of resistance of the stress sensitive resistor can be reduced by the simple addition of a parallel resistor of the proper value. Such a circuit is shown in Fig. 7. Thus, the transverse voltage strain gauge pressure transducer can be calibrated for zero pressure offset and full scale span and compensated for changes in offset and full scale span by using only passive components.

A calibrated, compensated pressure transducer using the transverse voltage strain gauge technology and the compensation and calibration techniques described above has been fabricated on a single silicon die. Figure 8 shows the errors due to span shift with temperature over the range of -40°C to $+125^{\circ}\text{C}$ of a transducer of this design, while Figure 9 shows the errors due to thermal offset shift. This type of device was fabricated by depositing thin film resistors on the transverse voltage strain gauge transducer die and using a thin film laser trimmer for adjusting the resistor values on the die. The deposition and patterning of thin film resistor materials is done with similar techniques and processes as the deposition and patterning of the metallization. The use of thin film resistor materials in monolithic integrated circuits is fairly wide spread. A detailed review of the types of materials used and the kinds of devices that are fabricated using these materials is given by Waits [11]. The laser trimming techniques used to fabricate this type of transducer are similar to the techniques used in the fabrication of monolithic high accuracy

16 bit analog-to-digital and digital-to-analog converters save that with the transducer the part is exercised over pressure. It is interesting to note that the device shown in Figures 8 and 9 was exercised over a limited temperature range in order to increase the accuracy of the trim that compensates for thermal offset shift. However, it is possible to fabricate devices that show errors of $\pm 1\%$ FS from 0°C to 85°C without having to change the temperature of the device during trim. Temperature excursions are not required in order to compensate the temperature dependence of full scale span. It is possible to trim this device and compensate for thermal shifts in offset and full scale span without exercising the part over temperature due to fact that it is a single resistive element which eliminates the problem of resistor mismatch [4] and that the offset is defined by a single photolithographic step, making it highly reproducible.

CONCLUSIONS

It has been found that silicon pressure transducers using the four terminal transverse voltage strain gauge technology can give very good performance characteristics. The sensitivity of these devices is comparable to those obtained using the more common Wheatstone bridge construction while offering several advantages. Because of the small size of the active area of this type of strain gauge, very small non-linearity errors can be achieved while maintaining high full scale span output voltages. Since the zero pressure offset voltage is determined by the same photolithography and diffusion steps used to fabricate the stress sensitive resistor, very good control can be achieved for this characteristic and its temperature coefficient. By using proper doping levels, temperature characteristics can be achieved which allow the temperature dependence of full scale span to be compensated using a single series resistor. A method has also been developed which allows for the fabrication of a compensation and calibration circuit on the same substrate as the pressure transducer using thin film resistor deposition and laser trimming techniques.

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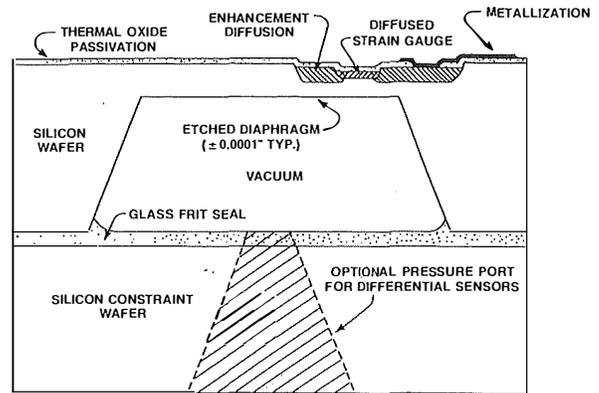


Fig. 1. Cross Sectional View of a Silicon Pressure Transducer

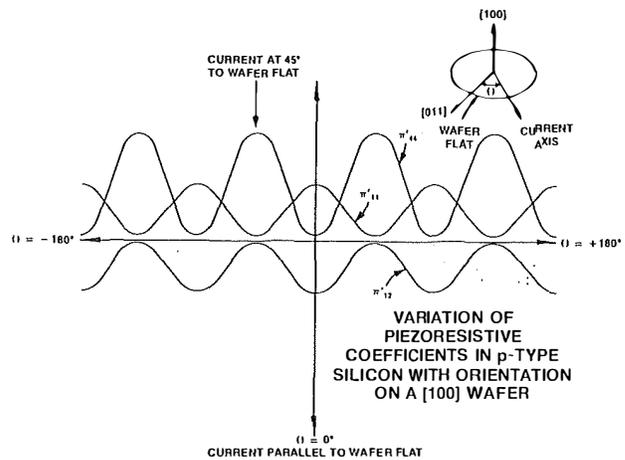


Fig. 2.

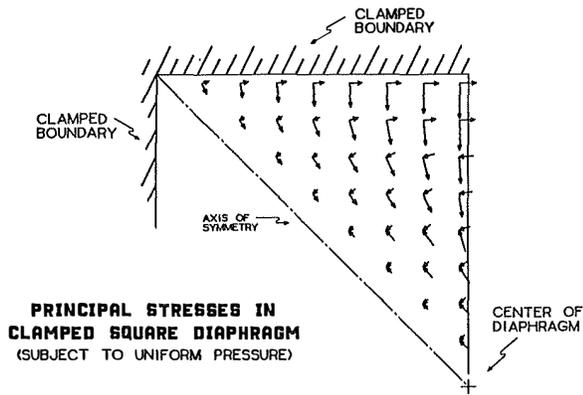


Fig. 3.

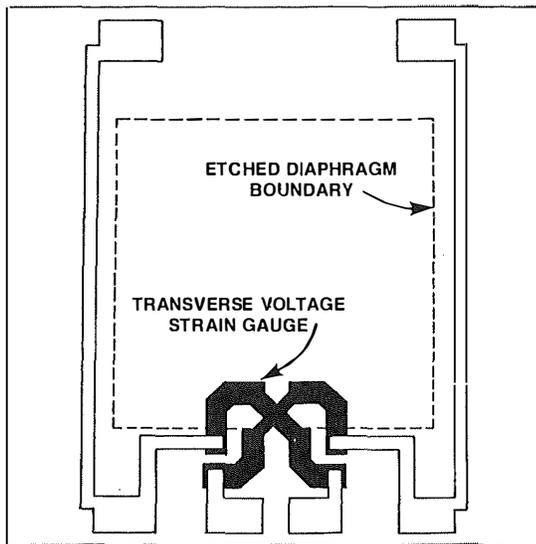


Fig. 4. Plan View of Motorola "X-ducer" Silicon Pressure Transducer.

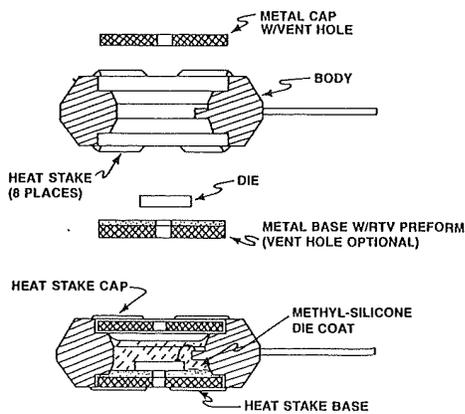


Fig. 5. Cross Sectional View of a Chip Carrier Pressure Transducer Package.

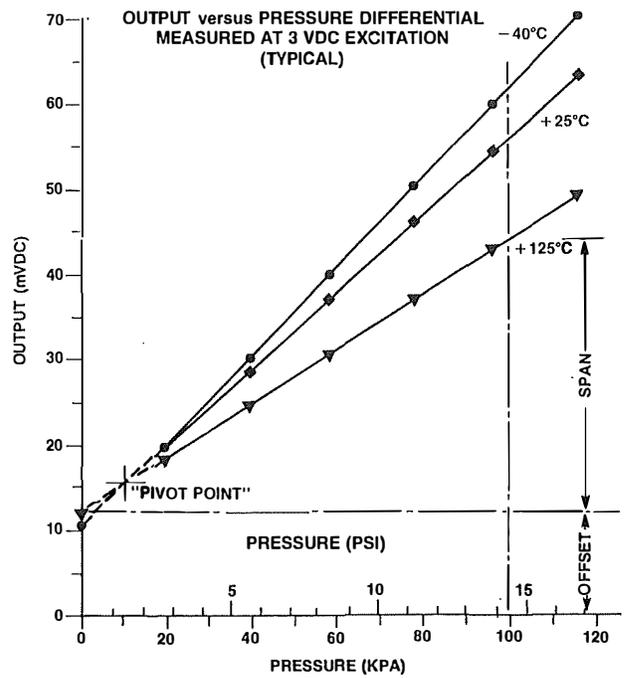


Fig. 6. Output of a Typical MPX-100 Pressure Transducer Demonstrating Temperature Dependence of Zero Pressure Offset and Full Scale Span.

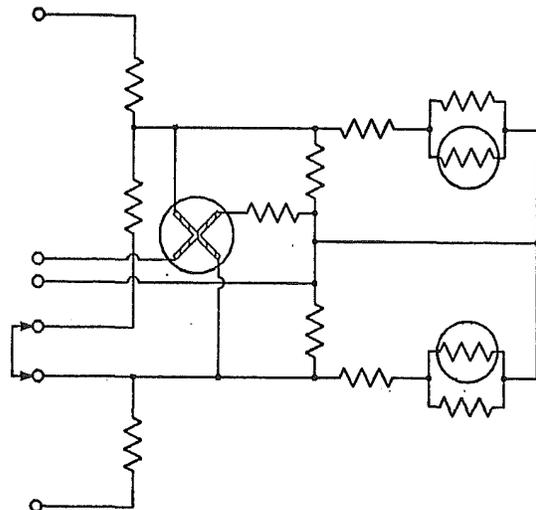


Fig. 7. Circuit Schematic for Compensation and Calibration of a Four Terminal Transverse Voltage Pressure Transducer.

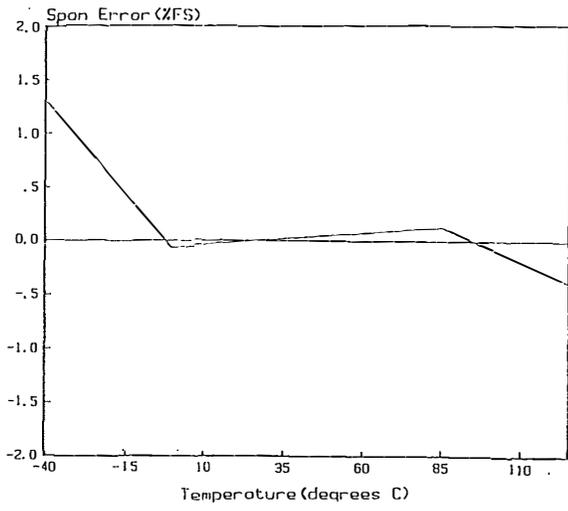


Fig. 8. Span Error vs. Temperature for a Pressure Transducer with On Chip Compensation and Calibration.

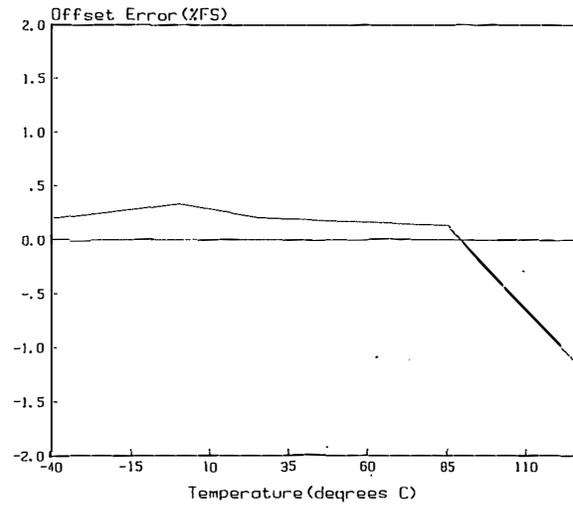


Fig. 9. Offset Error vs. Temperature for a Pressure Transducer with On Chip Compensation and Calibration.

AN IMPROVED MONOLITHIC ACCELEROMETER

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An improved 100g DC accelerometer is being developed. Prior monolithic accelerometers [1], [2] were not optimized for wide operating temperature range or maximum sensitivity for a given f_n . Present capacitive or piezoelectric designs [3], [4] are unable to measure static acceleration. An existing 100g Insouth design was used as a starting point for a new development effort. Design goals included: 1 mV/g sensitivity with 10 volt excitation, $f_n > 2$ KHz, low span error, low cross axis sensitivity, and $< 2\%$ bias over a temperature range of -65°C to $+95^\circ\text{C}$. The design would be capable of reasonable yields to produce a low cost unit.

The design approach utilized performance data from an existing Insouth accelerometer as a starting point for a factor change analysis. Cantilever equations relating f_n and ϵ to beam length, width, thickness and proof mass were decomposed into proportionalities as shown in Figure 1.

These proportionalities allow accurate design modification as well as flexibility to quickly trade-off parameter changes. The design goals required an increase in sensitivity and higher f_n than the previous accelerometer. It is obvious from Figure 1 that a simultaneous increase in f_n and ϵ (sensitivity) is impossible with any one parameter change. However, a two parameter change will allow both f_n and sensitivity to be improved. Reducing beam length should be used to raise f_n because the improvement of f_n occurs at a higher rate than the resulting degradation of sensitivity. Similarly, increased proof mass, and decreased width and thickness should be used only to increase sensitivity because ϵ (sensitivity) will increase at a higher rate than f_n degradation.

The final mechanical design shown in Figure 2 is a 54 x 63 mil die having a cantilever beam 500 μm wide and 575 μm long. The silicon proof mass is 500 μm x 500 μm at the top surface and 200 μm thick. In order to minimize beam length (measured to the center of mass) and maximize proof mass a material much denser than silicon is required for the proof mass. Gold preforms 20 x 20 x 3 mils were used on the improved accelerometer. The 3 mil thickness moves the center of mass of the composite proof mass up to the flexure plane and eliminates the moment that causes cross axis pickup. In addition to the improvement of cross axis rejection the added preform increases sensitivity by an order of magnitude.

The strain sensors are ion implanted or diffused piezoresistors. Sensor arrangements included a full active full bridge (FAFB) and a depletion MOSFET structure similar to a full active half bridge (FAHB). The 500 Ω FAFB is a conventional strain gauge bridge chosen for its simplicity and low impedance output. The same resistor layout rotated 90° is used for longitudinal and transverse elements of the bridge to prevent layout induced offset.

The 6 μm gate metal on the depletion MOSFET sensor is located on the beam flexure line where maximum ϵ occurs. The gates are intended to deplete the piezoresistor and increase its resistance in a region of maximum strain resulting in an electrically controllable $\Delta R/R$ enhancement. Since both MOSFET elements are gate controllable as shown in Figure 3, the output offset is also electrically adjustable.

The improved accelerometers were tested over temperature as well as mechanically characterized. The f_n of the units without gold proof mass is 7.8-8.5 KHz in good agreement with the calculated 7.46 KHz. Experimental test results for the FAFB with 10 volt excitation are given in Figure 4, and frequency response plots of accelerometers with and without gold preform mass are shown in Figure 5.

The MOSFET sensor was too heavily doped to saturate at low voltages. However, a $\Delta R/R$ enhancement was observed with positive gate bias. The effect of gate voltage on sensitivity is shown in Figure 6 for a 10 volt excitation and gate voltages from zero to 40V. The MOSFET sensor output vs. temperature can be varied with gate control and could be used as a temperature compensation method. Figure 7 shows the output change with temperature for gate voltages from zero to 10 volts and no acceleration applied.

Parameter	Relationship to Natural Frequency	Relationship to Maximum Strain
MASS	$f_n \propto \frac{1}{m^{1/2}}$	$\epsilon_{\text{max}} \propto m$
LENGTH	$f_n \propto \frac{1}{L^{3/2}}$	$\epsilon_{\text{max}} \propto L$
WIDTH	$f_n \propto w^{1/2}$	$\epsilon_{\text{max}} \propto \frac{1}{w}$
THICKNESS	$f_n \propto t^{3/2}$	$\epsilon_{\text{max}} \propto \frac{1}{t^2}$

Fig. 1. Table of Cantilever Proportionalities

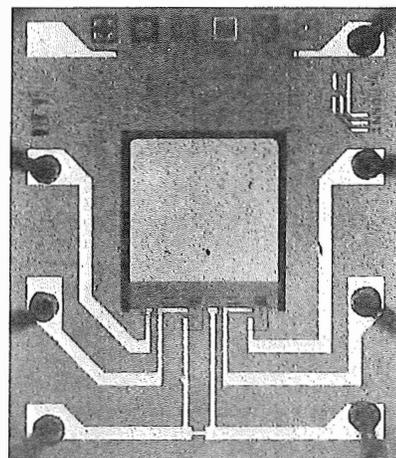


Fig. 2. Photograph of FAFB Monolithic Accelerometer

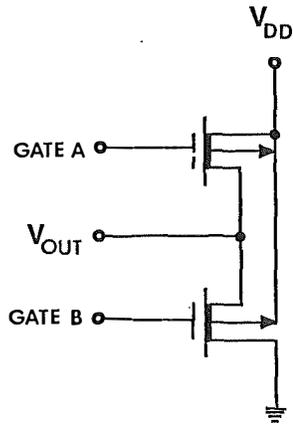
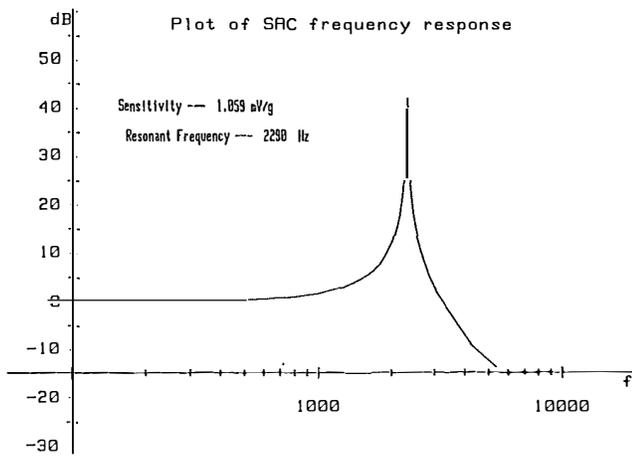


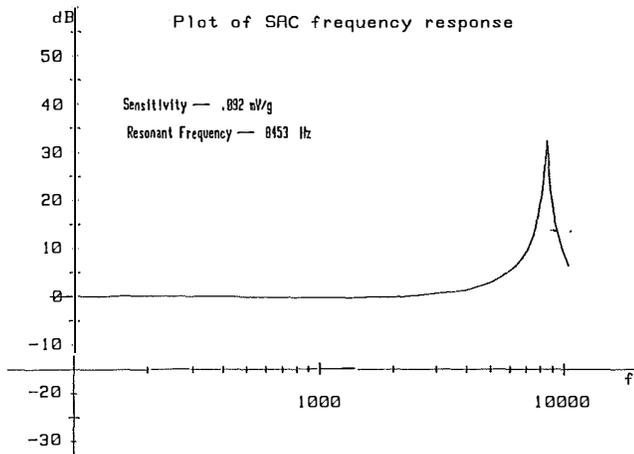
Fig. 3. Schematic of FAHB MOSFET Accelerometer

Scale Factor	.8 - 1.4 mV/g
f_n	2.4 KHz
Cross Axis Pickup	1% - 6%
Bias Over Temperature -65° + 95°C	3%
TCGF	<1100 ppm/°C
Non-Linearity	<5%

Fig. 4. FAFB Accelerometer Test Data



(a)



(b)

Fig. 5 Frequency Response of FAFB Monolithic Accelerometer.
(a) With Gold Proof Mass. (b) Without Gold Proof Mass.

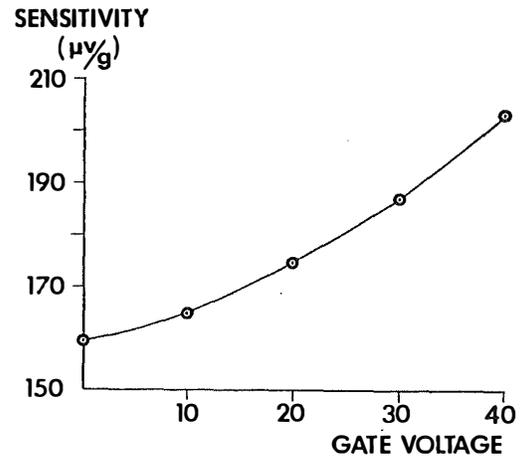


Fig. 6. MOSFET FAHB Accelerometer Sensitivity vs. Gate Voltage. Bridge Excitation was 10 Volts.

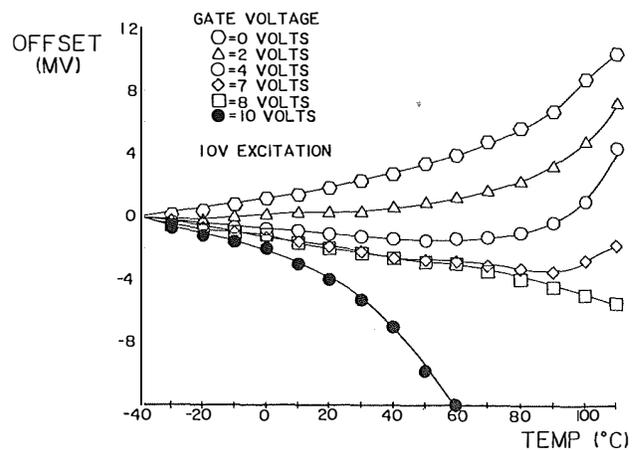


Fig. 7. MOSFET FAHB Output Offset Change vs. Temperature for Several Gate Voltages. All Data Taken with 10V Excitation and Referenced to -40°C Data Point.

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STANDARD MANUFACTURING PROCESSES FOR ADVANCED SILICON SENSOR FAMILIES

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INTRODUCTION

Just as in other developing technologies most of the principles involved in the fabrication of silicon micromechanical structures have been known for many years. Fundamental processing techniques unique to these structures include,

- anisotropic etching on (100) and (110) substrates (using KOH, EDP, and other etchants)
- isotropic etching (using various HF/HNO₃ acid mixtures)
- thin films for masking silicon etchants (primarily SiO₂, Si₃N₄, and Cr/Au)
- design of mask geometries to tailor the under-etched patterns in micromechanical structures
- doped layers in the silicon to stop and control etching (i.e. the p+ etch-stop for EDP and KOH, the preferential attack of heavily-doped silicon in some isotropic etchants, and the electrochemical behaviors of both these systems)
- epitaxial layers to control critical mechanical thicknesses
- dielectric isolation techniques for special high temperature applications
- anodic bonding of Pyrex to silicon for structurally supporting and hermetically sealing micromechanical structures
- glass frit and eutectic sealing (alternate methods for the same purposes)
- thermo-migration of aluminum in silicon to provide electrical feedthrus from one side of a wafer to the other and to fuse two wafers together
- etching of Pyrex glass to form complementary patterns in anodically-bonded structures

Although all of these techniques have already been incorporated in commercially available products, the full exploitation of micromechanical fabrication technology is far from being realized. Substantial evidence of this is apparent in the rapidly expanding number of papers in the field as well as in the overwhelming response to the announcement of this meeting.

THE ROLE OF INTEGRATED CIRCUITS

While micromechanical devices do require many unique thin film techniques such as those listed above, nevertheless, it is the principles of integrated circuit processing technology which have always been at the core of silicon micromechanics. From thermal oxidation, diffused resistors, epitaxial layers, aluminum metallization, and even packaging methods to the fundamental concepts of photolithography,

silicon-based mechanical sensor technology and silicon IC technology were originally established from the same background during the same time frame. Since the early 1960's, however, the IC industry has advanced through at least 5 product generations while silicon micromechanics is barely into its second generation.

Certainly the primary reasons for such a relatively slow development are economic as shown in Figure 1. The current DEMAND for large numbers of inexpensive, digital, smart-sensors could not have been initiated without the current PROLIFERATION of large numbers of inexpensive microprocessor chips.

Key to the continuing development of advanced silicon smart-sensors is the persistent exploitation of silicon IC technologies and methodologies... not only on the basis of higher integration levels, new thin film processes, and smaller line-widths but, just as importantly, on the basis of generalized, but versatile technology FAMILIES. In the same way that a single bipolar (or CMOS or NMOS) circuit process can support a large family of CIRCUIT products, it is possible to support a large family of smart-SENSOR products with a series of well-developed, standard micromechanical processes. Using these principles, new products are designed by applying well-understood design rules for a series of well-characterized process steps. As illustrated in Figure 2, a new mask set is generated, but the new product can be manufactured on an existing product line, along with other products in its family.

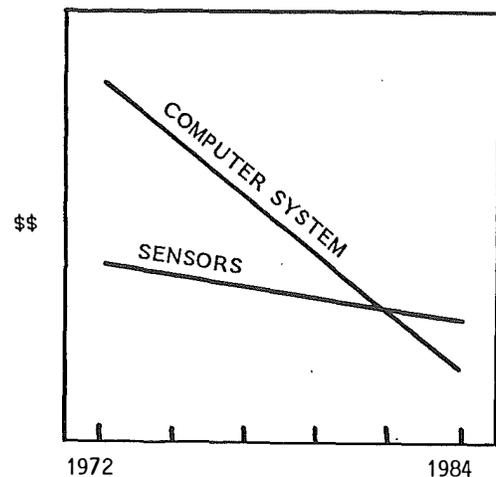


Figure 1

The intensive development of integrated electronics has resulted in plummeting costs of digital computers. Only recently have the costs of electronics dropped below those of sensors in computer-controlled systems. This turn of events has prompted an increased level of sensor development.

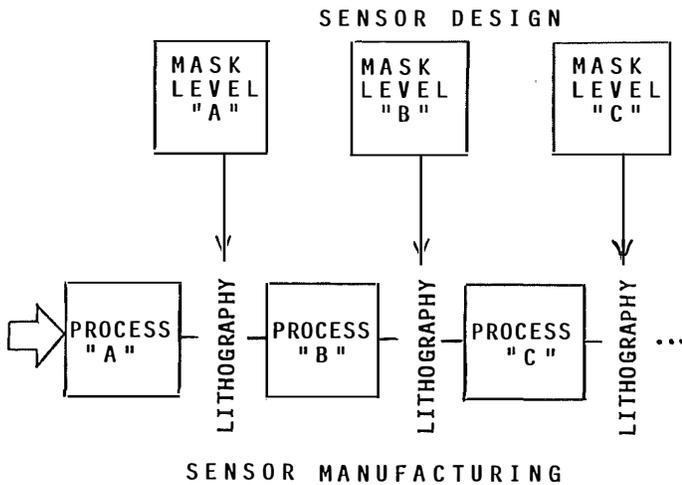


Figure 2

Just as in integrated circuit device families, advanced silicon sensor families can be based on standard manufacturing processes. Standard design rules are generated from these common processes which are then used to design a new mask set for each new sensor in the family.

Of course, such sensor families do currently exist to a limited extent, but the extension of these ideas to smart sensor families with on-board circuitry is a more demanding challenge. First of all, it is crucial to have an intimate knowledge of the details of the IC processes used in the circuit fab-line, as well as a basic understanding of the limitations of current circuit manufacturing technologies. As a general rule, for example, only limited pre-processing of a sensor wafer is acceptable prior to fabricating the circuits. Because of lithography and handling constraints, the very large topographies or unusual materials encountered in many types of sensors are steps which must wait until the circuitry is completed. In particular, pulling wafers out of a circuit fab-line, doing a special process, and re-introducing them midway through the sequence is even more frowned upon as illustrated in Figure 3.

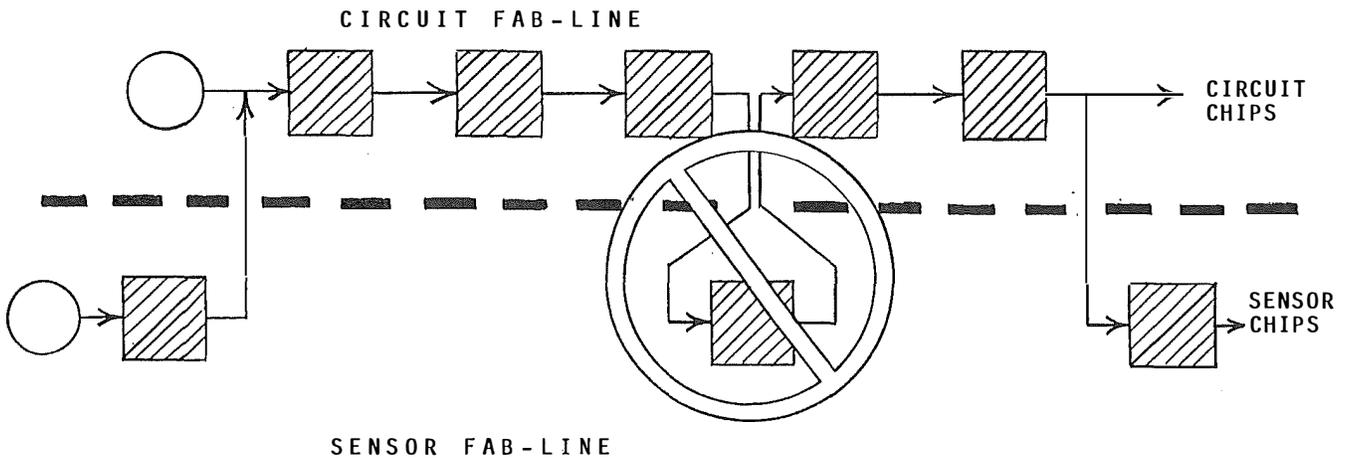


Figure 3

The processing sequence of a circuit fab-line should not be interrupted to perform special processing functions for sensors. This may compromise the circuit performance, yield, and/or reliability. Instead, special processing steps must be implemented prior to the start of circuit fabrication (these steps are very limited) or after complete circuit fabrication.

Once a circuit processing sequence is established its optimum performance, yield, and reliability will only be maintained by following these considerations.

IC-COMPATIBLE SENSOR STRUCTURES

Integrated circuitry immediately adjacent to sensing devices and structures has the potential for enormously increased detection sensitivity and noise immunity in all types of sensor transduction techniques. In addition, design and processing costs for low-volume integrated circuit chips continue to drop with the proliferation of CAD tools and custom silicon foundry services. It is inevitable that on-board integrated circuits will be increasingly employed in silicon-based sensor families. One basic approach to the smart-sensor family relies on the concept of hermetically sealing the circuitry - on a wafer scale - underneath Pyrex glass or another silicon wafer, similar to the structures first demonstrated by Sanders and Knutti (1), Lee and Wise (2), and Ko, Bao, and Hong (3). Advantages to be expected from this approach are:

- circuitry is well-protected from the environment;
- the assembly is thermally matched;
- circuitry is also well-protected from subsequent etching steps for a wide range of sensor-related microstructures;
- packaging is simplified because a significant part of the packaging function is accomplished on the wafer level.

Such advantages are certainly not without development problems:

- hermetic sealing of circuitry within a small volume;
- hermetic, low resistance, well-insulated electrical feedthrus;
- bonding and sealing must be performed on a wafer scale;
- and all of these requirements must be completely compatible with established circuit technologies.

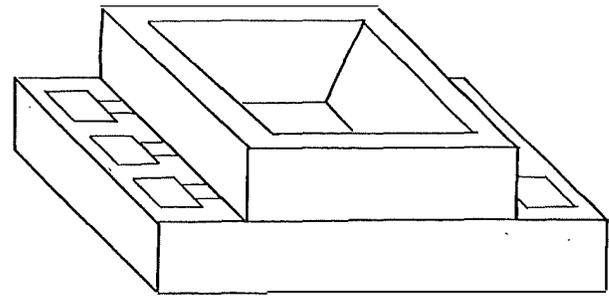
Each of these issues, complex problems by themselves, are made all the more difficult by being closely coupled. For example, high reliability, hermetic, wafer-scale bonding is very sensitive to surface topography, while IC topographies and various proposed electrical feedthru techniques are notorious for generating unacceptably large surface features.

Since this approach can resolve the common, long-standing pursuit of optimal circuit passivation and protection, the potential benefits are impressive. As shown in Figure 4, the concept is applicable to many types of silicon-based sensors, including pressure, temperature, force and chemical. It also provides a convenient separation between the sensing and circuit functions.

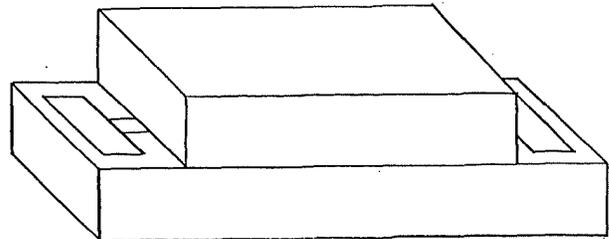
It seems that the many diverse aspects necessary to effectively commercialize silicon micromechanics, silicon micromachining, and silicon-based smart sensors are now in line. As described earlier, the proliferation of computers has supplied both the technical foundation and the economic impetus. In addition, there is now a critical mass of people working in these areas as well as a critical mass of technical literature. Finally, a number of highly successful commercial products have been identified which can serve as catalysts to increasing development efforts. The practical implementation of these concepts will greatly influence the next generations of miniature mechanical structures, physical sensing devices, and the important sensor/computer interface.

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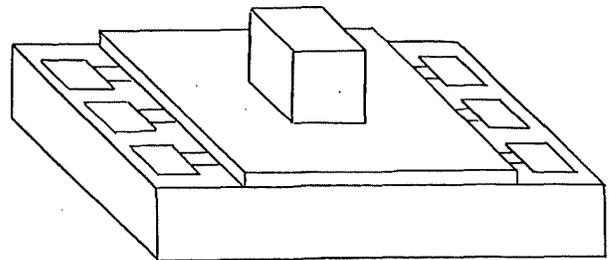
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A) PRESSURE



B) TEMPERATURE



C) FORCE

Figure 4

Examples of transducer structures from a proposed "smart-sensor" family with circuitry hermetically sealed between two chips.

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Abstract

The most highly developed of solid-state sensors are visible image sensors. Visible image sensor arrays with more than a million picture elements and with noise levels in the tens of electrons have been developed. In this paper the architectures of image sensors are reviewed, and the key issues are discussed. As an example of the present status of sensor technology, results on a 360,000-pixel charge-coupled image sensor are presented.

Sensor Architectures

The first visible image sensor array was reported in 1967 [1]. However, the development of present-day sensors occurred after the discovery of the charge-coupled device (CCD) in 1970 [2]. The first applications for solid-state sensors were in military and commercial systems. Most of these sensors were linear arrays. More recently, area arrays have been developed for consumer applications. Owing to the continuing development of process technology for silicon integrated circuits, the cost of solid-state imagers is rapidly becoming competitive with the electron-beam-scanned camera tubes such as the saticon. Sensor arrays with 180,000 pixels are in production, and arrays with 360,000 pixels are in advanced development. The advances in silicon VLSI technology that made large-area arrays feasible have also made possible linear arrays with up to 5732 elements [3,4], high-sensitivity time-delay-and-integrate (TDI) scanners [5], very high-frame-rate imaging arrays for high-speed video photography [6], and very high-resolution arrays for astronomy [7].

An image sensor consists of photosensitive elements that convert the incoming light to charge and readout structures that transfer the charge to the output. Three major classes of photosensitive elements are in wide-spread use: the photodiode, the photocapacitor, and the photoconductor. The structure and band diagrams for these photosensitive elements are illustrated in Fig. 1. The photodiode consists of a p-n junction. Usually the implantation for the photodiode is tailored to yield a high electric field from the surface to aid in collection of photoelectrons generated near the surface, giving a high blue sensitivity. Owing to the low capacitance of the diode structure, the charge storage capacity of the photodiode is usually small. For image sensor array applications, the diode is usually fabricated in a p-well to reduce crosstalk and blooming. A variant on the photodiode is the p^+n -p photodiode [8], in which a heavily doped p^+ layer is placed near the surface and the n-type layer is lightly doped and is fully depleted during operation. The p^+n front junction results in a factor of 5 or more charge capacity, as compared to the normal photodiode, as well as reduced image lag.

The photocapacitor consists of a thin polysilicon gate above an oxide. Owing to the high optical absorption of the polysilicon, the quantum efficiency is lower than in the photodiode, particularly in the blue. The photocapacitor is used most widely in the form of a frame-transfer CCD or the CID, although

photocapacitor arrays have been used for very high-speed applications [6]. Owing to the high capacitance of the MOS structure, the photocapacitor has the highest charge of all the photosensitive elements.

Recently, there has been great excitement over the development of photoconductive films such as hydrogenated amorphous silicon (α -Si:H) [9]. These films, deposited on top of an interline or X-Y-addressed diode array, result in a vertical integration of sensors. The α -Si:H photoconductors consist of a back contact (such as aluminum) that contacts the diode in the underlying array, an α -Si:H layer $\sim 1 \mu\text{m}$ thick, and a transparent top electrode. The photoconductor is biased to complete depletion. Photo-generated carriers are swept out of the photoconductor and stored in the underlying diode. The photoconductor offers high quantum efficiency, very high area utilization, and internal antiblooming.

The major classes of readout architectures for image sensors are the frame-transfer CCD [10,12], the interline-transfer CCD [13-16], and various X-Y-addressed MOS photodiode arrays [6,9,17-20] (Fig. 2). The frame-transfer CCD consists of an illuminated imaging area with vertical registers to integrate and transfer the charge, a storage register to store the charge during readout, and a horizontal transfer register. For television applications both the image and storage areas store one field (242 lines for NTSC television). Vertical interlacing is accomplished by integrating under different electrodes during the two fields, accomplishing a half-pixel shift in the relative position of the pixel. Frame-transfer CCD's have been constructed with two and three levels of polysilicon as well as with one level of polysilicon in virtual-phase CCD's [10]. Since the entire pixel area is photosensitive, the quantum efficiency is very high. However, absorption of blue light in the polysilicon electrodes reduces the blue efficiency. At the end of each field, the integrated charge must be transferred from the image to the storage register. This transfer, which typically requires almost a millisecond, results in some vertical image smearing owing to the very low capacitance of the CCD output ($<40 \text{ fF}$); the CCD has very low noise and hence very good low-light-level performance. Output noise values of $<50 \text{ rms electrons}$ at video rates have been reported.

The interline CCD imager consists of vertical CCD registers used for charge transfer and photodiodes for light sensing and charge storage. For NTSC television there would be 484 diodes vertically and 242 stages of the CCD shift register. At the end of one field the charge from the top diode in each stage is transferred onto the vertical CCD register, while in the other field the charge from the bottom diode is transferred. The vertical registers are optically shielded with aluminum. Owing to the separation of light-sensing and charge-transfer functions, the photodiode typically occupies only 25-40% of the cell area. This results in a lower overall quantum efficiency as compared to the frame-transfer CCD. However, use of photoconductive layers overlying the sensor could greatly reduce this disadvantage.

The unit cell of MOS X-Y-addressed imagers consists of a photodiode (or photocapacitor), a transfer

gate, and a diffusion contacted by a metal signal line. The transfer gates are addressed by a vertical scan generator, usually a dynamic shift register, which addresses each row sequentially. Horizontal charge readout may be accomplished with horizontal signal lines connected to the vertical signal lines by FET switches controlled by a horizontal scanner. Other X-Y-addressed arrays utilize a CCD for horizontal readout. Owing to the use of a metal signal line instead of a CCD for vertical transfer, the MOS array has a larger fraction of each pixel devoted to the photodiode, resulting in higher quantum efficiency. The MOS array is also simpler to manufacture. However, the sensitivity of the MOS imager at low light levels is severely constrained by the KTC and the pattern noise of the high-capacitance horizontal and vertical signal lines. Although the use of a horizontal CCD reduces the horizontal readout noise, the KTC noise of the vertical signal lines results in a factor of 10 higher noise than the interline CCD readout.

A 360,000-Pixel Solid-State Image Sensor

Sensor Design

As an example of the performance of present solid-state sensors, a 360,000-pixel charge-coupled image sensor will be described [11]. The sensor is used for imaging color photographic negatives on television, which places some unique demands on a solid-state sensor. These include wide dynamic range, low pattern noise, high resolution, and excellent color reproduction.

The sensor architecture is shown in Fig. 3a. The sensor consists of a four-phase CCD image area, dual two-phase horizontal registers, and separate output amplifiers for each of the three colors. During the vertical retrace interval the photographic negative is illuminated. The vertical clocks are held constant to integrate the signal charge. At the end of the vertical retrace interval the signal is read out. A row at a time is transferred into the horizontal registers. The charge from columns with green color filters is transferred to the top register, while the charge from the alternate columns with red and blue color filters is transferred to the bottom register. The dual horizontal register design was required to achieve the 12- μm horizontal column spacing without a third level of polysilicon. The horizontal registers are read out at a 7.15 MHz pixel rate. The charge is sensed by floating diffusion outputs and buffered by dual-stage buried-channel source followers. The use of dual-stage source followers allowed optimization of the first stage for low input capacitance and the second stage for high drive current. The use of the buried-channel FET design reduced low-frequency (1/f) noise.

A photomicrograph of the image sensor is shown in Fig. 3b. The image area is 8.8 mm (H) x 6.6 mm (V). A schematic of the pixel is shown in Fig. 3c. The channel-stop region is 2 μm wide, and the buried channel is 10 μm wide. The gate oxide under both the first and second polysilicon electrodes was 1600 Å thick, to maximize optical transmission in the blue. The polysilicon layers were both 1700 Å thick. Source-drain regions were formed by shallow arsenic implantation to minimize short-channel effects in the output structure.

Spectral Response

In a color image sensor in which the photosensitive area is fully covered by polysilicon, careful choice of the polysilicon thickness is required to achieve adequate transmission in the blue while

maintaining sufficiently low resistance to transfer charge vertically. Figure 4a shows the optical absorption coefficient of polysilicon as a function of wavelength. Figure 4b shows the measured spectral response of the sensor along with the response calculated from the known layer thicknesses and the optical constants. At wavelengths below 500 nm the response is dominated by optical absorption in the polysilicon electrodes. Between 500 and 800 nm the response is dominated by structure due to optical interference within the polysilicon and the gate oxide. Beyond 800 nm the light is absorbed well below the silicon surface, and the spectral response decreases, owing to recombination of the photogenerated electrons.

Organic color filter arrays are fabricated on top of the sensor in an R-G-B-G stripe geometry. The color filter arrays are processed by sequential coating, patterning, and dyeing of special photoresists developed for this application. Owing to the narrow (2 μm) light-shield width, extreme resolution and sharpness requirements are placed on the resist materials. The dyes for this color filter array were specifically designed for imaging photographic negatives.

Charge Capacity

Because of the large density range of photographic negatives, a wide dynamic range is required in the sensor. There are two limitations to charge capacity in a buried-channel CCD: (1) the interaction between electrons and interface states at the Si-SiO₂ surface and (2) the potential difference between well and barrier electrodes. Figure 5a illustrates the first limitation. The electrostatic potential and the electron density are shown as a function of depth for three different quantities of charge in the channel. As more electrons are added to the channel, the barrier to the surface decreases and the electron concentration at the surface increases. Electrons can be captured at interface states when electrons come in contact with the surface.

Owing to the narrow channel width, two-dimensional effects significantly reduce charge capacity. Figure 5b shows the electrostatic potential and electron distribution in two dimensions calculated by finite-difference techniques. The electron distribution is shown at the transition between buried- and surface-channel operation ($\phi_{\text{CH}} - \phi_{\text{S}} = 300 \text{ mV}$) for a $1 \times 10^{12} \text{ cm}^{-2}$ buried-channel dose. The electrons occupy only the center 4 μm of the 10- μm channel. For a $2 \times 10^{12} \text{ cm}^{-2}$ buried-channel dose with a significantly larger barrier between channel and surface, the electrons occupy the center 7 μm of the 10- μm channel. The barrier between the electrons in the channel calculated as a function of the electron density is shown in Fig. 5c for two buried-channel doses using one- and two-dimensional models. Figure 6 shows the experimentally measured differential charge-transfer inefficiency for the image area as a function of the number of electrons per pixel for the two buried-channel doses. The $1 \times 10^{12} \text{ cm}^{-2}$ dose yields a capacity of 100,000 electrons per pixel, and the $2 \times 10^{12} \text{ cm}^{-2}$ dose 800,000 electrons, in good agreement with the two-dimensional model.

Noise

The noise sources in this sensor include pattern and shot noise from dark current, output amplifier noise, and photosensitivity pattern noise due to the sensor and the color filter array.

The dark current in better sensors at room temperature was 5 nA/cm^2 or 1600 electrons per pixel. Measurements of the dark current in test structures adjacent to the sensor as a function of gate voltage showed that surface generation accounted for 2.5 nA/cm^2 , generation in the buried-channel implanted region for 1 nA/cm^2 , generation in the unimplanted portion of the depletion layer for 0.5 nA/cm^2 , and diffusion current for 0.1 nA/cm^2 . Comparison of test structures with and without channel stops indicated that the channel stops contributed an additional 1 nA/cm^2 to the overall dark current. Subsequent analysis by transmission electron microscopy revealed dislocation loops 100 \AA in diameter in the implanted region of the channel and precipitates 50 \AA in diameter in the channel-stop regions.

The largest random noise source is the output amplifier at 200 rms electrons per pixel in a 3.5-MHz bandwidth. The output amplifiers are two-stage buried-channel source followers with sensitivity of $2 \mu\text{V}/\text{electron}$. Owing to the use of buried-channel transistors in the source follower and to double correlated sampling in the signal processing, the output amplifier noise is almost entirely a result of thermal noise in these transistors.

In Fig. 7 the signal and the noise from various sources are plotted as a function of the density of the photographic negative. The largest noise source is the output amplifier noise at 200 rms electrons per pixel. The dynamic range of the sensor is 70 dB. This exceeds the dynamic range required for imaging photographic negatives.

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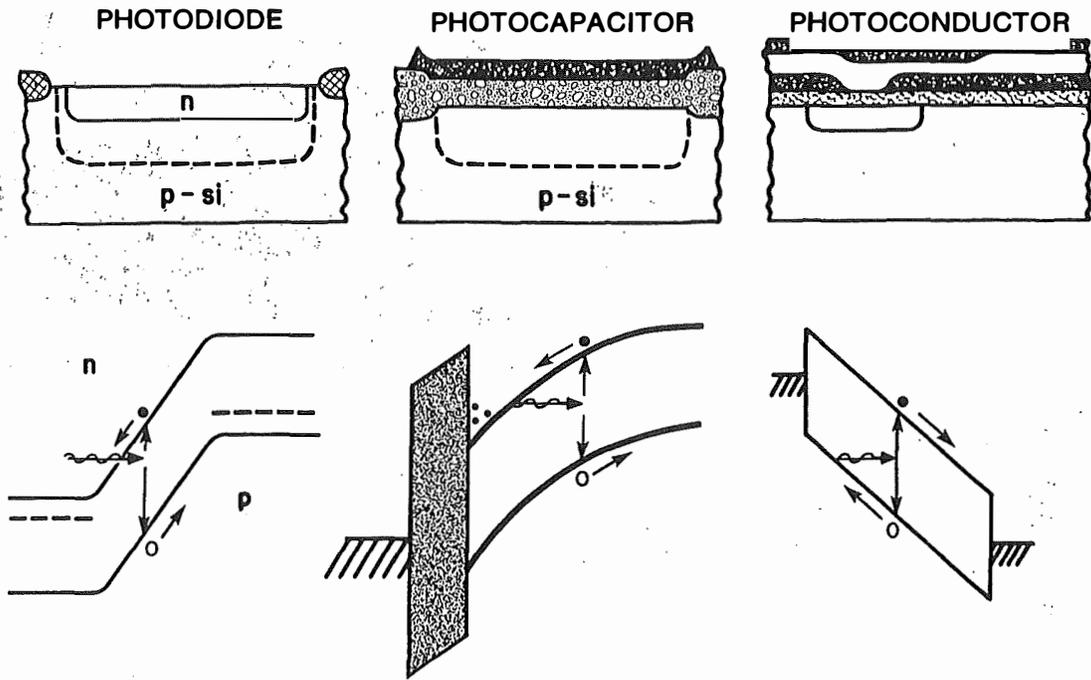


Fig. 1 Cross-sections and band diagrams of photosensitive elements: (a) photodiode, (b) photocapacitor, (c) photoconductor

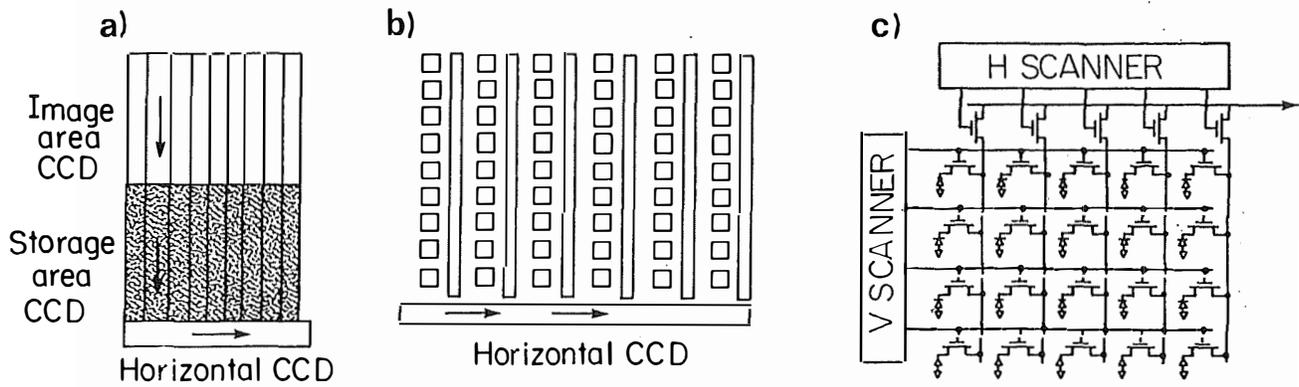


Fig. 2 Architectures of major sensor designs: (a) frame-transfer CCD, (b) interline-transfer CCD, (c) MOS diode array

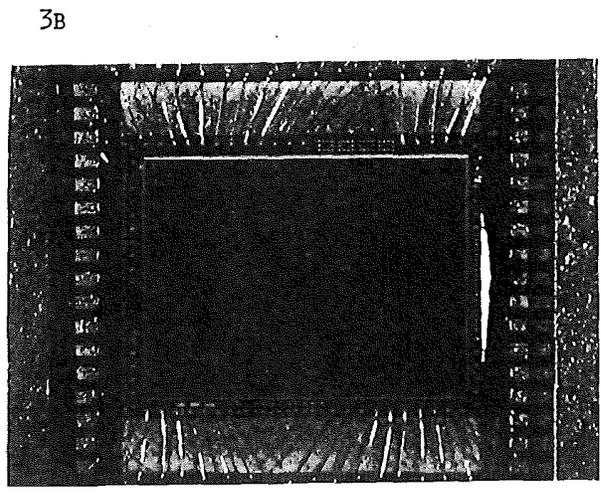
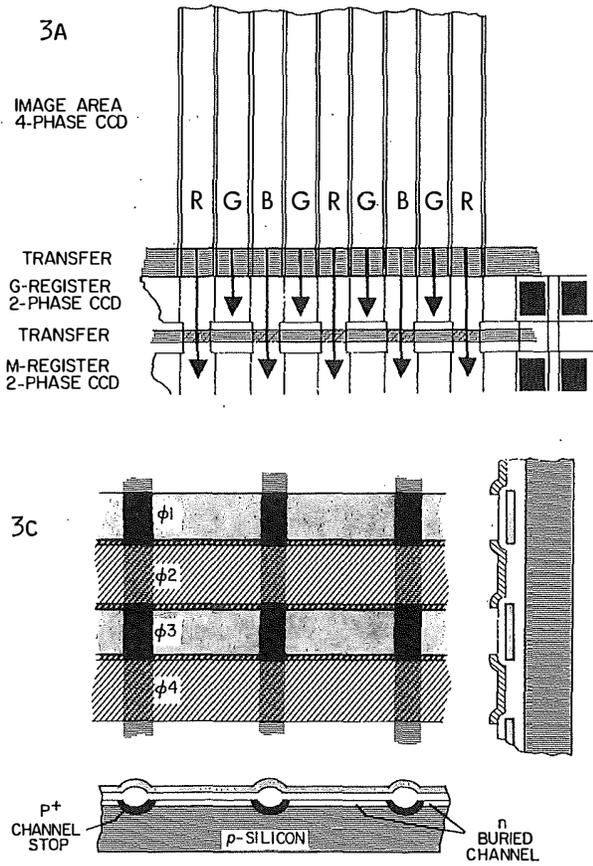


Fig. 3. (a) Design of image sensor. Sensor has 740 columns horizontally with R-G-B-G stripe color filter pattern. Vertical registers are four-phase C.C.D.'s; horizontal registers are two-phase.

(b) Photograph of sensor chip. Image area is 8.8 mm (H) x 6.6 mm (V).

(c) Design of image area. Width of column is 12 μm , including 2 μm channel stops.

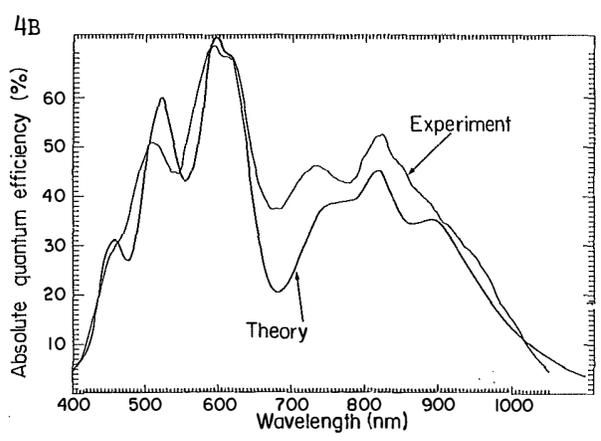
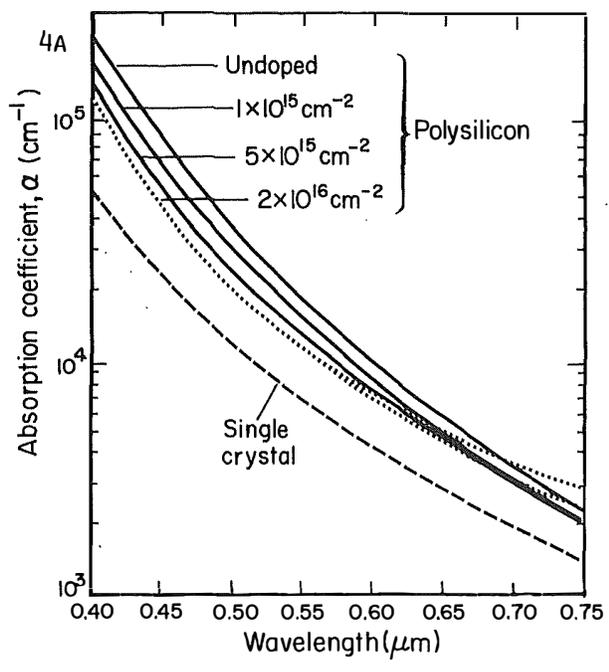


Fig. 4. (a) Absorption coefficient of polysilicon phosphorus doped at various concentrations.

(b) Measured and calculated spectral response of sensor.

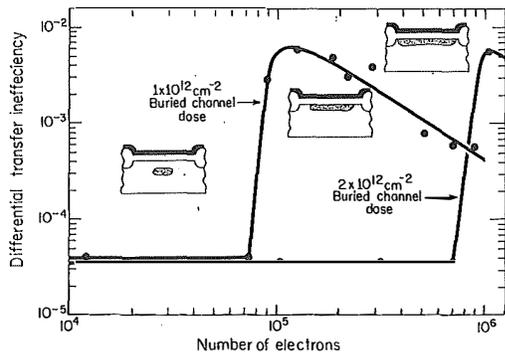
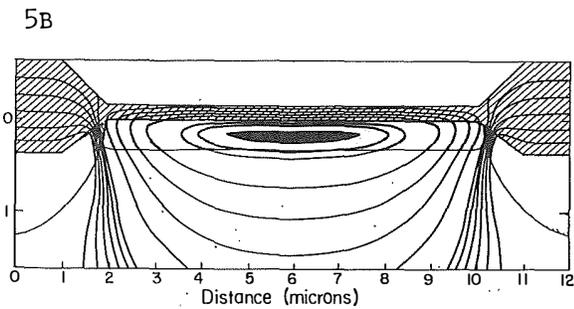
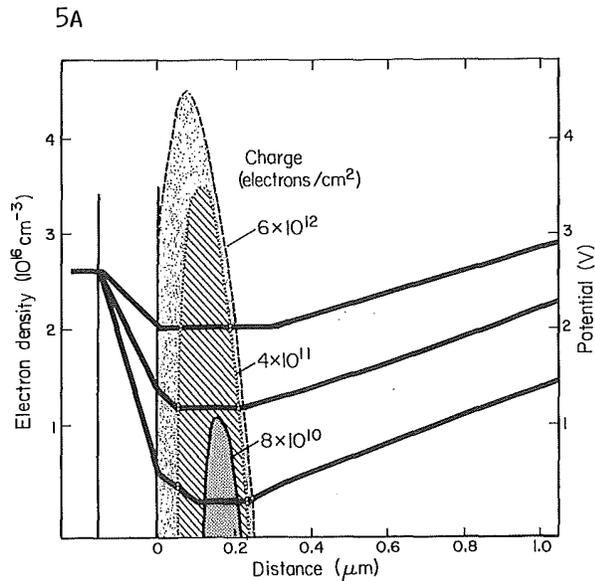


Fig. 6. Differential transfer inefficiency vs. number of electrons per pixel for vertical C.C.D. registers for two buried-channel doses.

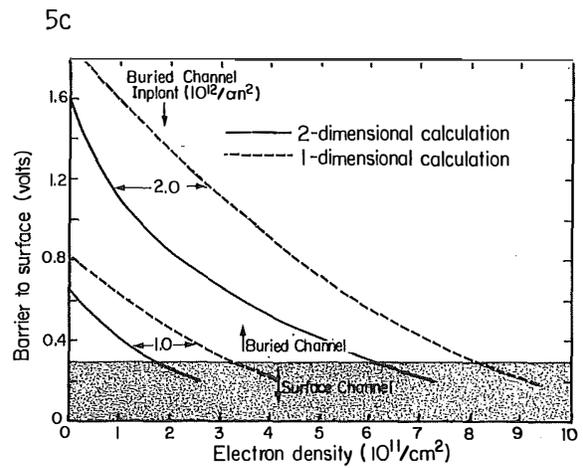


Fig. 5. (a) Electrostatic potential and electron distribution for different quantities of charge in the buried channel.

(b) Electrostatic potential and electron distribution in two dimensions for $10 \mu\text{m}$ wide buried channel.

(c) Potential barrier between buried channel and surface as a function of electron concentration for two buried-channel doses. Results of one- and two-dimensional models are shown.

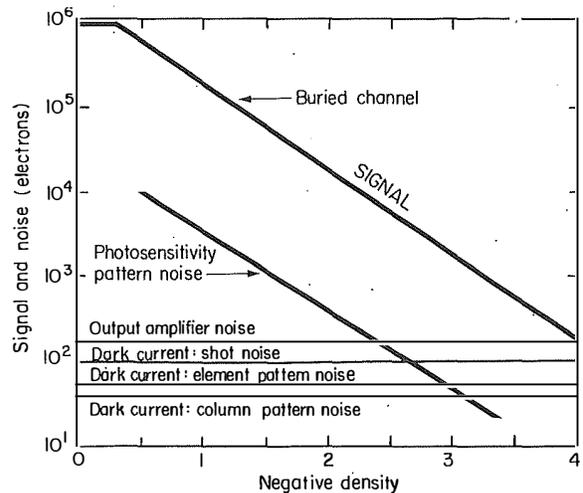


Fig. 7. Signal and noise as a function of the density of the photographic negative. Dynamic range of the sensor is 70 dB.

Monolithic Silicon Fabrication Technology for Flexible Circuit and Sensor Arrays

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Abstract

Arrays of circuit elements are fabricated on the surface of a silicon wafer and are interconnected by gold metallization. A layer of polyimide is then formed on the wafer surface by spinning on a layer of polyamic acid and curing it at high temperature. Masking and etching from the backside of the wafer leaves separate silicon islands supported on a flexible polyimide substrate, interconnected by the flexible gold metallization. Size is smaller than tape-bonded hybrids. Applications include linear thermometer arrays and two-dimensional arrays of sensors for robotic and biomedical uses.

Introduction

This research has been driven by the need to measure temperature profiles in living tissues during hyperthermia treatment of cancer. To measure such profiles, some minimally invasive means of inserting arrays of thermometers into a tumor is necessary [1]. Such thermometer arrays should have low thermal conductivity for accurate temperature measurement, and should be physically pliable and small in size for minimum tissue trauma during patient movement. They should also be fairly inexpensive to fabricate for low cost in clinical use. We previously developed a hybrid assembly technique to fabricate linear arrays of six thermometers which were small and flexible [2], but these arrays proved to be too difficult to fabricate in volume, and were not durable enough for in-vivo use.

We have developed a new, totally monolithic method of fabricating linear arrays of twenty silicon diodes which act as thermometers. The technology results in separate silicon islands supported on a thin, flexible polyimide substrate. Gold wires encased in the polyimide provide electrical interconnection of the islands. To date only passive silicon diodes have been fabricated on each island, but the technology can be used to fabricate transistors and active signal processing circuitry. The fabrication techniques are simple and preliminary yield data is good.

Fabrication Process

The method of fabrication runs as follows:

1. Use conventional integrated circuit techniques to fabricate circuit elements on one surface of a silicon wafer.
2. Interconnect the circuit elements with thin gold leads. We use 1 micrometer thick gold with an adhesion layer beneath the gold, and a diffusion barrier in the device contact holes.
3. Spin on an adhesion promoter to make polyimide stick to silicon dioxide. Spin on a layer of polyamic acid, and slowly raise the wafer temperature to 350 C to imidize the polyamic acid and form a polyimide layer. The diffusion barrier mentioned in the preceding step is necessary to prevent alloying of the gold with the silicon at the 350 C cure temperature.

4. Open holes in the polyimide layer over contact pads on the wafer frontside.
5. Mask and etch the wafer backside in a hydrofluoric acid/nitric acid mixture, forming separate silicon islands. The metal lines are exposed at this point, and are supported by the polyimide substrate.
6. Add more polyamic acid on the wafer backside and cure to 350 C. This step encases the silicon islands and gold leads in a solid layer of polyimide.
7. Cut out individual arrays with a scalpel.
8. Test and package the arrays.

The structure of a flexible array is illustrated in Figure 1.

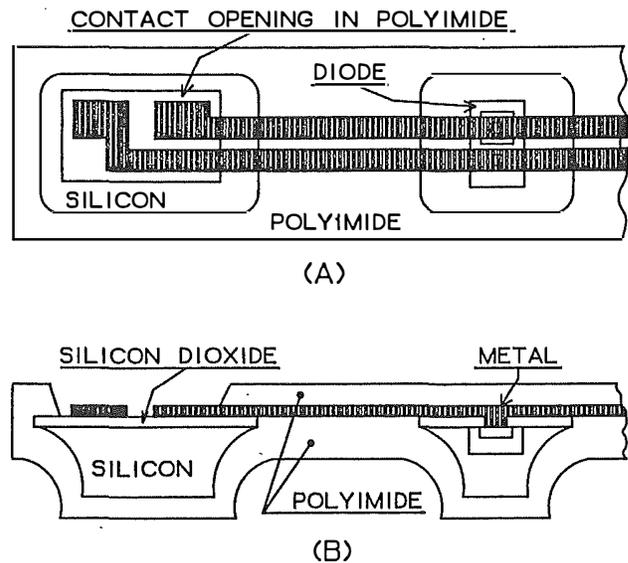


Figure 1: Flexible array. (a) Plan view, (b) Cross-section.

Application to Thermometer Arrays

Three versions of linear thermometer arrays are under development. 3.5-cm long arrays of twenty diodes have been fabricated on 5-cm diameter silicon wafers, tested, and packaged. These arrays are useful test vehicles but are too short for most clinical applications. On 7.5-cm diameter silicon, 10-cm and 20-cm long arrays are being fabricated as of this writing. The 10- and 20-cm arrays are long enough for use in most human tumors.

The interconnection technique for the diodes in the 3.5-cm arrays has been explained previously [2], and allows the use of $N \times (N-1)$ sensors on N wires (in this case, 20 diodes on 5 wires). Our present mask set allows fabrication of 22 of the 3.5-cm arrays on a 5-cm silicon wafer. For the 10-cm and 20-cm arrays we have modified the multiplexing technique for a 4-terminal measurement at each diode to reduce any errors due to resistive drops along lead wires. The modification results in doubling the number of lead wires, giving 10 leads for a 20-diode array.

To allow 10-cm and 20-cm arrays to be fabricated on a 7.5-cm diameter wafer, it is necessary to form the arrays on the wafer as a meandering shape. During the final assembly and packaging process, the meandering shape can be slit to the proper shape with a scalpel, folded out to form a long linear array, and glued at the folded joints to make it hold its shape. We are presently fabricating six of the 20-cm arrays plus four of the 10-cm arrays on each 7.5-cm diameter wafer.

All three types of thermometer arrays are small enough to be inserted into hollow needles or catheters, or glued onto a needle or other probe, for insertion into tissue. Packaging techniques are still under development.

Acknowledgements

This work is supported by the Biotechnology Resources Branch of the NIH Division of Research Resources under grant P41-RR-01086. We owe special thanks to Krishna Saraswat, whose LPCVD tungsten solved our metal problems.

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CHEMICAL MICROSENSORS FOR VAPOR DETECTION

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The detection and monitoring of vapors is an important problem in such areas as process control, chemical hazard assessment, and environmental analysis. Unfortunately, many traditional solutions to the vapor monitoring problem have involved sensors which are large and expensive (e.g. IR spectrometers, Gas Chromatography/Mass Spectrometry, etc.). Thus the cost of chemical concentration information has been very high. This has resulted in a terrible bottleneck in the application of ever cheaper microcomputer technology to a vast array of process control, and environmental monitoring problems. Chemical microsensors can eliminate this bottleneck.

In their most general form, chemical microsensors consist of at least two elements: a microfabricated physical probe device and a chemically selective coating. The probe device contacts the coating and provides an electrical signal whose characteristics reflect the state of the coating. The coating is in contact with the medium in which the chemical species are to be detected. Variations in the coating properties through chemical and physical interactions, modulate the transport of matter or energy through the probe device. Work at NRL has focused on probe devices in which the transport of electrons, acoustic waves, and electromagnetic waves is modulated by chemical interactions.

The modulation of acoustic waves is accomplished using a coated Surface Acoustic Wave (SAW) delay line oscillator. Thin polymer coatings have been investigated theoretically and experimentally for their ability to selectively detect a variety of vapors. Sorption of the vapor into the coating increases the mass of the film and reduces the velocity of the Rayleigh surface wave. This is detected as a reduction of the resonant frequency of the delay line oscillator. Rapid and reversible detection of many vapors at the part per million concentration level and below has been demonstrated. A typical response of a 31 MHz SAW water vapor sensor to consecutive pulses of 5 ppm water is illustrated in figure 1.

The modulation of electronic charge transport through thin organic semiconductor films is observed with a device called a Chemiresistor. The device consists of an interdigital microelectrode array (usually gold) fabricated on an insulating substrate (usually quartz). This microelectrode is then coated with a thin organic semiconductor film. Ohmic contacts are obtained with phthalocyanine films. Interesting results have been obtained with thin sublimed films of various metal substituted phthalocyanines but the best results have been obtained from ordered multilayer films prepared by the Langmuir-

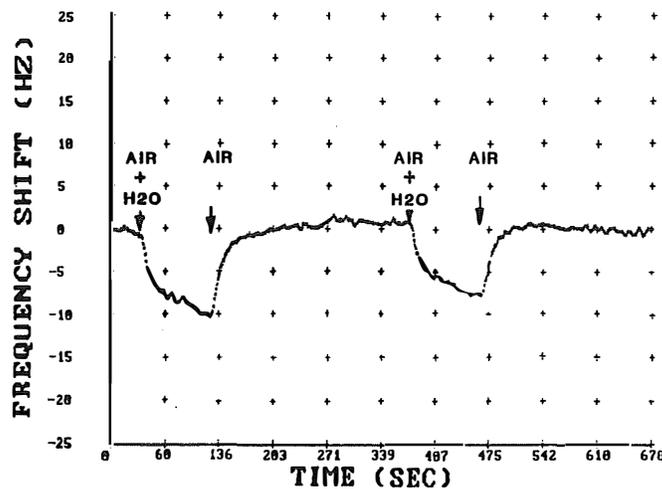


Figure 1. Typical response of a polymer coated 31 MHz SAW device exposed to consecutive pulses of 5 ppm water vapor in dry air.

Blodgett technique. Very fast, sensitive, and reversible responses to electron donor gases are common. A typical response of a copper phthalocyanine L-B film to 2 ppm pulses of ammonia is illustrated in figure 2.

At this time the key technical challenge is to improve sensor selectivity. Efforts at NRL have emphasized chemical design, synthesis, and characterization of selective coatings, along with precise film deposition methods. The use of pattern recognition techniques with array sensors may ultimately result in a system comparable to the human nose in its ability to detect and identify vapors.

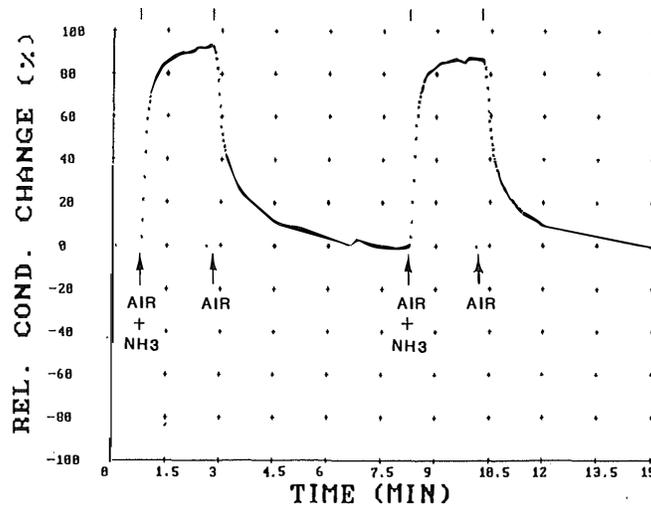


Figure 2. Response of a derivatized copper phthalocyanine multilayer film chemiresistor exposed to consecutive pulses of 2 ppm ammonia in dry air. (Starting conductance = 9×10^{-13} ohms⁻¹).

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Chronically implantable neural information sensors are designed to transduce electrical potentials from the central or peripheral nervous system. The purpose of developing this technology is to eventually provide information to control assistive devices for the physically disabled. The technology will potentially benefit a variety of disabled individuals such as amputees and spinal cord injury patients.

Current research focusses on the design and fabrication of the structure used to interface electrical systems with nerve tissue. The following discussion highlights some of the important design considerations involved in the development of this technology.

Neural activity consists of 250 microsecond current pulses (action currents) which flow through active cell membranes into extracellular spaces surrounding cell bodies and axons in the nervous system. Current density at the active membrane surface is approximately $.01A/cm^2$ [1]. The action currents create potential gradients (action potentials) which can be sensed by electrode contacts in the extracellular space. The electrode arrays in figures 1 and 2 can be used to sense such potentials.

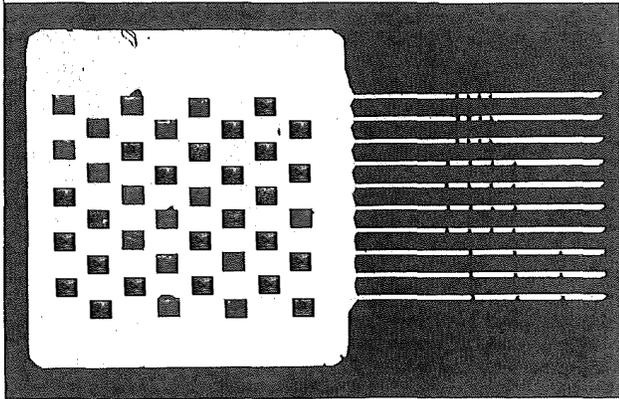


Figure 1: Insertable 40 contact electrode array.

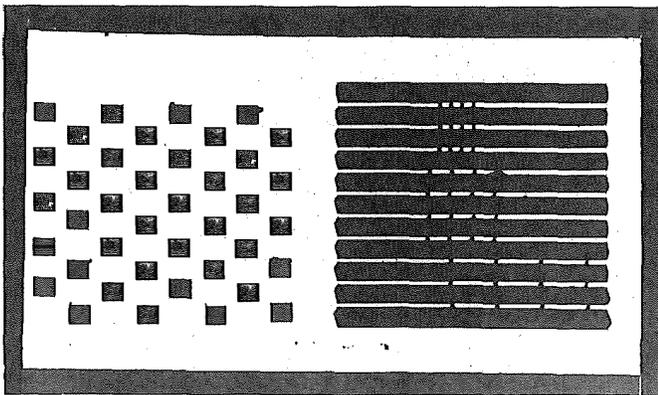


Figure 2: Regeneration 40 contact electrode array.

These arrays were chemically machined from (110) silicon substrates. The silicon bars are 40 microns wide and 40 microns thick. Each bar is 2mm long and carries four electrode contacts spaced from 100 to 400 microns apart. The bars are spaced 200 microns apart. Four micron wide, phosphorus doped polysilicon conductors connect the bonding pads with the electrode contacts. Polysilicon conductors were necessary to reduce thermal stress which can induce crystal defects in the etched silicon bars near the end of the conductors.

Implantable electrode arrays must be biocompatible and must be able to withstand immersion in corrosive physiological environments indefinitely. The metal system used on these arrays was selected after evaluating a number of potential systems in heated, oxygenated Ringer's solution [2]. Tantalum was used to form a stable, ohmic, Ta-TaSi-Si contact. A platinum layer formed a stable, oxidation resistant interface to the tantalum. The outer metal was gold which was the most biocompatible metal available. The gold was deposited with sufficient surface energy to enhance nucleation and produce a micro-rough surface. The micro-rough surface reduced the magnitude of the electrode/electrolyte impedance to $340M\Omega-\mu^2$ at 1Khz. A combination of LPCVD silicon nitride and APCVD silicon dioxide was deposited to insulate the conductors.

The biocompatibility of the structures has been verified in the peripheral nervous system and the cerebral cortex of rabbits [3,4]. Biocompatibility is a relative term. Certainly, devices which produce gross inflammatory response are not biocompatible. Devices which may not cause obvious inflammatory response but which cause neuron cell death are not biocompatible. The definition is less obvious, however, when the degree of connective tissue encapsulation of the implant is considered. All physical structures implanted in mammalian systems are encapsulated by varying thicknesses of connective tissue. This connective tissue displaces the cells being sensed from the electrode contacts which reduces signal amplitude and electrode selectivity. Thus the degree of connective tissue encapsulation is of critical importance because it influences design of the electrode contacts themselves.

Cortical Electrodes

Electrode contact area is the primary design variable which can be optimized for signal, noise and selectivity. In the cerebral cortex, the activity of neuron cell bodies is of interest. There are approximately 24,000 cell bodies per mm^3 in the cortex. The cortex is 1.5 to 4.5 mm thick. Cell diameters range from 6 to 70 microns in the cortex [5]. Simple analyses assume that these cells represent spherical current sources in a homogeneously conductive medium. The maximum potential seen at the surface of a cell membrane relative to a distant reference is given by:

$$V_{max} = pJr_s$$

where: p = effective resistivity of the medium
 J = membrane current density
 r_s = radius of the cell

According to this simple analysis, a 1.5mV potential should be seen at the surface of a 15 micron radius cell in a 100Ω-cm medium assuming a membrane current density of .01A/cm².

Under the above assumptions, potentials from action currents can be shown to vary as 1/distance from the center of the source. The potential seen by a point contact in the medium is given by:

$$V = \frac{\rho J r_s^2}{r}$$

where: r = radial distance from effective center of the source.

The actual spacing of the neuron cell bodies from the electrode contacts is determined by the electrode orientation and the amount of encapsulation by glial cells. Recent biocompatibility tests of the insertable electrode array have shown that a 5 micron microglial cell layer typically encapsulates the array.

A point contact on the electrode array located 5 microns from a 30 micron diameter cell would be expected to sense a 1.1mV potential during the peak of an action potential. A 6 micron cell for the same conditions would generate a potential of 110μV.

The electrode contact area does not significantly influence signal amplitude as long as electrode contacts are relatively concentric with the equipotentials. However, noise and selectivity are inverse functions of electrode size. The choice of appropriate electrode size then depends on acceptable noise versus acceptable selectivity. The larger the electrode area, the more likely it will overlap significant potentials from adjacent cells. Exactly how large an electrode can be depends on required signal differentials for the instrumentation, cell sizes and spacing, and connective tissue thickness.

Maximum selectivity can be achieved by minimizing the geometric electrode area until electrode impedance becomes the limiting factor. Since minimization of electrode area maximizes the number of electrodes possible on a given structure, setting the electrode area on the basis of electrode impedance levels is a reasonable approach. (It should be noted here that the degree of selectivity appropriate for neural prostheses is not well defined at present. Less selective electrodes have the advantage of integrating activity from several related sources which may improve efficiency of data acquisition considerably). At present, it appears that the peak to peak noise level of the input electrodes should be less than 20 microvolts to avoid signal degradation. A plot of noise versus electrode radius for the rough gold system is shown in figure 3.

From this analysis, a minimum electrode area of 150 μ² would be required to satisfy noise requirements. An electrode which was 12x12 microns should easily record from 6u diameter cells spaced 5μ from the electrode plane (effective diameter = 16μ). Such an electrode would be expected to generally sense activity from one or two closely spaced 6u cells, but up to three cells could conceivably create significant potentials on the electrode. It is likely that such selectivity is adequate for most practical purposes at present.

An electrode area of 150μ² would be expected to have an impedance of 2.3 Megohms at 1 kHz. The presence of such a high source impedance is the primary driving force for integrating circuitry onto electrode structures used for chronic implantation.

Peripheral Nerve Electrodes

In the peripheral nervous system, activity from myelinated axons is of interest for control of prostheses for amputees. There are roughly 10⁴ axons/mm² arranged longitudinally in bundles to form peripheral nerves. Activity from these axons can be sensed near active membrane nodes. Nodes are 1 micron wide swaths of electrogenic membrane which encircle the nerve at longitudinal spacings of 300 to 3000 microns.

The regeneration electrode structure in figure 2 can be used to sense activity from these nodes [2]. Transected peripheral nerves grow through the slots in the implant. The electrode contacts lie transversely oriented to the axons. This results in a weak relationship between electrode radius and recorded potentials. Because of the minimum of 10 microns of connective tissue encapsulation observed during biocompatibility testing, nodes cannot be closer than 10 microns to any contact. Since internodal spacing is 300-500 microns in regenerated rabbit peripheral nerve, the probability that a particular axon node will be located within ten microns of the plane of the electrode array is about .025. Relatively few axons would be expected to yield maximal signals on a given electrode contact with this design. Electrodes tend to be selective, then, because of this random spacing of nodes relative to the electrode plane.

In spite of uncertainties in absolute values, some insight into the design of electrode contacts for the regeneration arrays for peripheral nerves can be gained by performing an analysis with an idealized model of the system [2]. The results of such an analysis (figure 3) point out that noise may limit the usefulness of an electrode configuration, and that there is a minimum size requirement for electrode contacts. This is because signal amplitudes are a weak function of electrode radius while peak electrode thermal noise is inversely proportional to electrode radius.

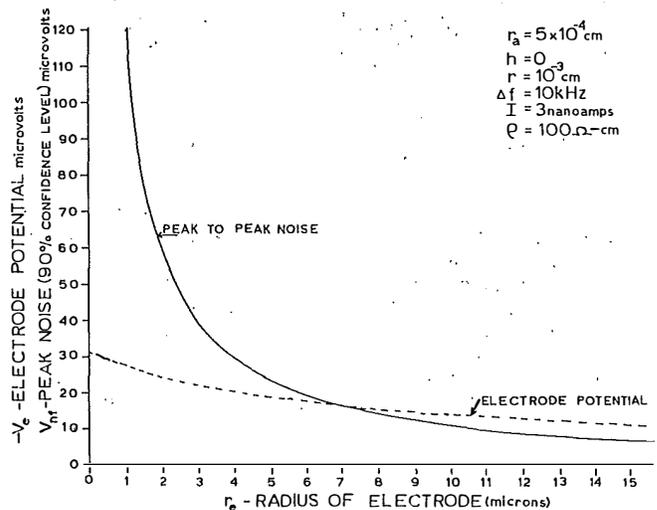


Figure 3: Electrode potential and peak noise as a function of electrode radius for rough gold metallization.

Experimentally, the maximum recorded potentials (figure 4) are an order of magnitude larger than predicted by a model which assumes a homogeneous medium.

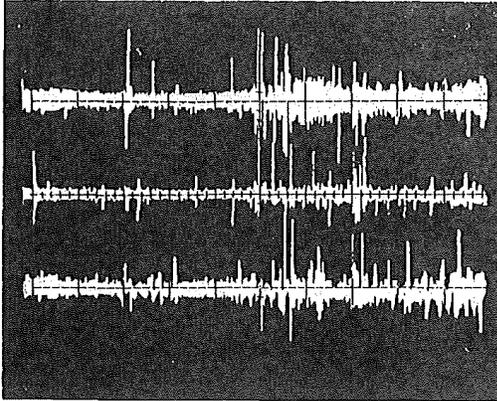


Figure 4: Three sets of differentially recorded peripheral nerve activity from a chronic silicon implant. Scale - Vertical = 500 μ V, Horizontal = 200msec

There are several possible explanations for the discrepancy. Histological analysis revealed that near the implant, fibroblasts formed hollow tubes which encircled small groups of axons (figure 5).

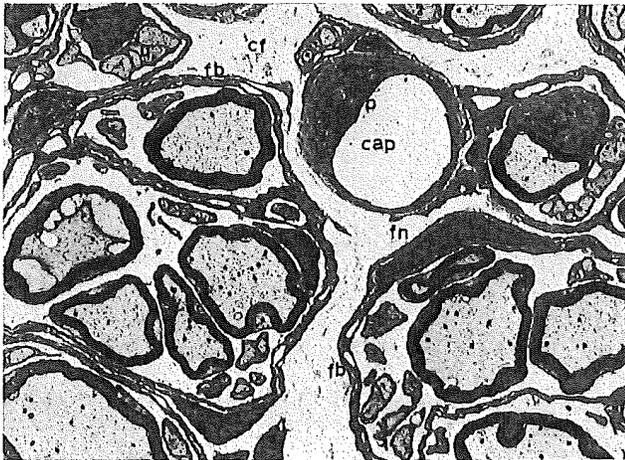


Figure 5: TEM of cross section of rabbit peripheral nerve which regenerated through a silicon grid one year earlier (2850x).

If these sheaths constrict the flow of action currents, then very large potentials may be observed within the tubes. Electrodes which do not intersect the sheaths would be expected to yield smaller signals than predicted. Electrodes which are connected to the sheaths may exhibit much larger potentials depending on the electrical properties of the elements and the structure of the connection. At this time, the electrical nature of these connective tissue sheaths is unknown.

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DEVELOPMENT OF AN IMPLANTABLE MICRODIELECTROMETRY SENSOR[†]

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Microdielectrometry is a sensor-based method for the measurement of low-frequency dielectric and conductive properties of relatively weakly-conducting materials such as resins, plastics, adhesives, rubber, thin films, and dielectric oils [1,2]. The sensor is a silicon integrated circuit that includes an interdigitated electrode pair, matched FET's, and a diode temperature sensor. The measurement instrument in its most recent form includes digitally generated excitation signals and synchronous digital extraction of response parameters using Fourier transform methods [3]. This paper reports the development of a sensor/package combination that permits the Microdielectrometry probe to be used in a wide variety of materials-processing environments, including chemical reaction vessels and laminating presses.

The sensor/package combination is based on flexible circuit-board concepts. The sensor chip is fabricated in NMOS silicon-gate technology, and is laid out so that the eight bonding pads are at one end, the transistors toward the middle, and the electrodes at the other end (actually occupying 3/4 of the total chip area) [4]. The chip size is 2.5 x 5 mm. The sensor package is fabricated out of laminations of copper and Kapton[®], each layer with its own pattern. The lower Kapton[®] layers have space for the entire chip, while the topmost layer has two openings, one for the interdigitated electrodes, the other for the contact pads. The copper layer is etched into eight leads that overhang the pad opening and register with the chip pads.

The packaging procedure is, first, to bond the chip to an adhesive carrier layer, second, position the package and affix it to the adhesive layer, third, form the eight wire bonds, and, fourth, fill the bond pad opening with an epoxy resin which, when cured, encloses the bonds and active device regions. The final thickness of the chip/package combination is 0.45 mm. The flexible ribbon cable portion of the package which connects the chip to the electronics can be as long as 40 cm, and is 0.15 mm thick. The sensor can drive an additional 3 meters of cable, if required.

Sensors packaged in this manner have been successfully inserted into chemical batch reactors for reaction end-point determination, and have been laminated into epoxy-glass circuit boards and other composite laminates for cure monitoring at temperatures up to 250°C and at pressures up to 1000 psi.

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SENSOR APPLICATIONS OF PERMALLOY THIN FILMS

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Sensors utilizing permalloy thin films have been developed for measurement of temperature, current, proximity and air flow. These sensors utilize the resistive and magnetoresistive properties of permalloy. Their design, construction and performance will be described and compared to some well-known technologies in each sensing area.

Permalloy is attractive for magnetic sensing because the full scale change in magnetoresistance is developed for fields on the order of 50 gauss or less. The sensitivity facilitates the construction of proximity sensors capable of detecting very small targets, and allows the design of current sensors which utilize simple flux collectors. Another important feature of permalloy (81% Ni, 19% Fe) is that it has no magnetostriction, minimizing concerns regarding stress sensitivity induced by packaging the sensors.

The magnetoresistive properties of permalloy have been known for many years. With the development of permalloy thin film techniques, it is now possible to construct low cost, batch processed sensors using this technology. The magnetoresistive effect $\Delta R/R$ in permalloy is on the order of 2.5% for a 50 gauss field, adequate to construct useful sensors. The magnetoresistive effect in permalloy is shown in figure 1. The resistance is a maximum when the applied field is zero and decreases as the magnetic field is increased. Note that this function is symmetrical about the zero gauss axis. Using the magnetoresistance effect in AC applications, therefore, requires that a bias field be applied to avoid a two-valued output. The magnetoresistive effect is also nonlinear, (approximating a \cos^2 function), so that constructing linear sensors poses significant problems.

One approach to constructing a permalloy linear current sensor is through the use of a rebalance scheme. A simple flux collector constructed from a strip of permalloy formed into a circular shape contains multi-turn rebalance coils. The conductor carrying the current to be measured is passed through the flux collector. This sets up an applied field which is sensed by a permalloy bridge. The electrical signal thereby generated is amplified and applied to the rebalance coils. Thus, this sensor operates at a fixed point on the permalloy magnetoresistance function, making its non-linearity inconsequential. Another approach is the use of geometries for the permalloy elements which linearize the characteristic.

Less well known is the fact that permalloy can be used for temperature sensing, providing the same sensitivity as platinum with higher base resistances and at lower cost. The resistance vs. temperature characteristics of permalloy and platinum are compared in figure 2.

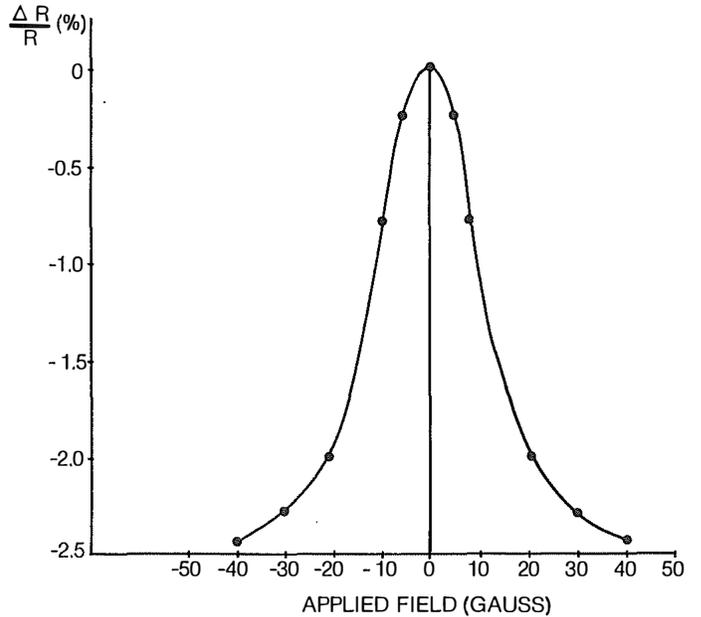


Fig. 1: Magnetoresistance In Permalloy

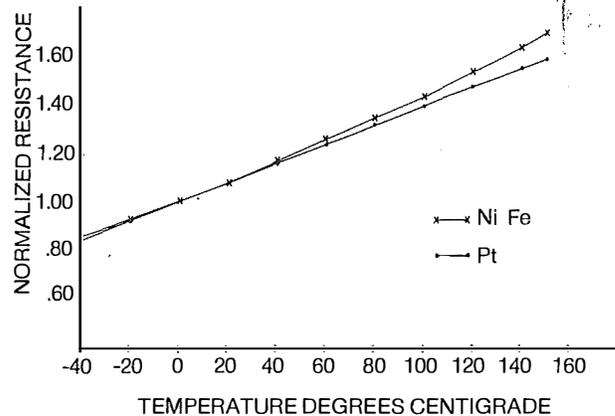


Fig. 2: Resistance vs. Temperature Comparison Of Permalloy & Platinum

Careful design reduces magnetic sensitivity to negligible levels. Relatively thick films approach the bulk properties of permalloy, yielding consistent TCR characteristics. Laser trim is used to standardize the room temperature resistance to a $\pm 0.15\%$ tolerance, making the devices interchangeable.

By mounting the temperature sensor on a ceramic with a low-value laser-trimmed thick film resistor (used as a heater), a simple air flow sensor results. With constant power applied to the heater, increasing air flow reduces the temperature (and resistance) of the sensor. The temperature of the air flow sensor is given by $T = T_H + T_A - fV$, where T_H is the temperature rise due to the heater resistance, T_A is the ambient temperature, f is a non-linear function relating resistance to air velocity, and V is the velocity of the air flow. Another temperature sensor placed in the same air flow allows the effect of ambient temperature (T_A) to be removed. The resistance vs. air velocity characteristic of this device is illustrated in figure 3.

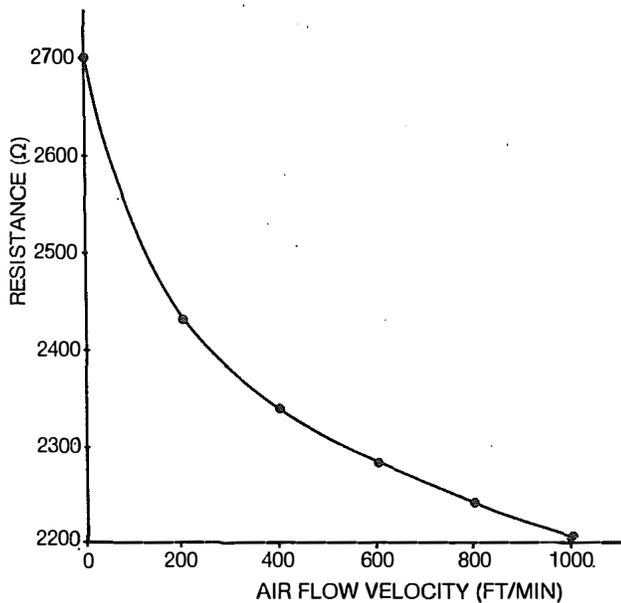


Fig. 3: Resistance vs. Air Velocity Characteristic Of Air Flow Sensor

The common thread in the sensors just described is their utilization of permalloy thin films to achieve improvements in the performance vs. cost spectrum. Finally, bipolar or CMOS signal conditioning electronics may be placed on the same die with the thin film sensor, resulting in fully integrated sensors.

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The need for hysteretic devices capable of high temperature operation arises in several areas of industrial process control. These devices could be incorporated in the circuit design for sensors and actuators, or could be used as memory elements which serve to identify the equipment in which they are employed.

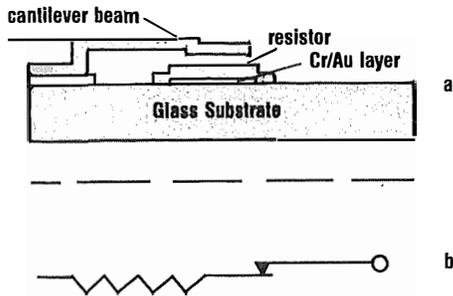


Figure 1

In Figure 1, a candidate device called an H-switch (hysteretic switch) is shown in a cross section view along with an equivalent circuit diagram. The conception of the H-switch was greatly influenced by the work of Nathanson [1] and Petersen [2]. As can be seen, an H-switch is a metal cantilever beam suspended over a thin film resistor. Metallization provides electrical contact to the base of the switch and to the lower side of the intercontact resistor. The resistor plays the important role of providing the device with hysteresis. With a small voltage applied to the contacts, an electric field is established between the cantilever and the surface of the resistor. This field exerts a force on the beam, deflecting it toward the resistor. An equal but opposite restoring force is provided by the elastic properties of the cantilever itself. As the applied voltage is increased, the electric field increases, deflecting the beam further. The electrostatic force increases inversely with the square of the distance between the beam and the resistor, while the restoring force varies linearly with the displacement of the beam from its equilibrium position. As the voltage is increased further, a critical point is reached where the spring force exerted by the beam is no longer able to overcome the electrostatic force. The beam suddenly closes on the resistor, making electrical contact. At this point, the voltage required to hold the switch closed is far exceeded by that applied. Therefore, to reopen the switch, the voltage must be lowered considerably.

The ideal H-switch current-to-voltage (I/V) characteristics are illustrated in Figure 2. The voltage at which the switch closes, V_{on} , is determined by the geometry of its design. For

example, a switch with a longer cantilever beam will close at a lower voltage if all other parameters are held constant. The voltage at which the switch will reopen depends, among other things, on the thickness and dielectric constant of the intercontact resistor.

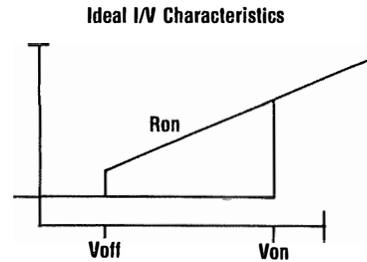


Figure 2

While a two-terminal device has conceptual simplicity, the same I/V characteristics can be achieved with a three-terminal device, such as shown in Figure 3. In this case, the function of the intercontact resistor is replaced by an external resistor connected between the field plate and the contact. In this way, fabrication difficulty is significantly reduced and reliability is increased.

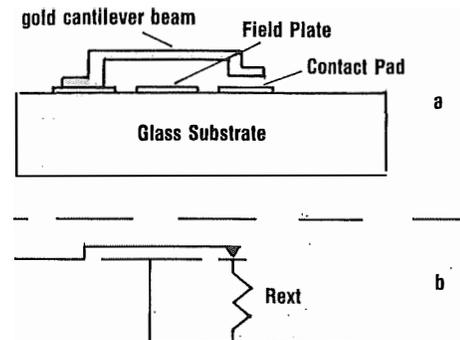


Figure 3

H-switches have been fabricated on glass substrates using the following process steps. A chrome/gold (500Å/2000Å) layer is E-beam evaporated on a Corning 0211 Glass Substrate and subsequently patterned and etched. The resistor layer is deposited and patterned so as to cover the counter electrode completely. Sputtered films of silicon and evaporated films of germanium make suitable resistor layers. The layers must be thick enough to withstand the electric field that will be applied when the switch is closed. In most of our work, we

found that one or two micron layers were more than adequate. Next, a "spacer" layer of between one and four microns of nickel or copper is deposited. After patterning, the spacer layer is etched to open holes through to the base contact region. Finally, the wafer is patterned to the plating mask with a positive resist (AZ1350J, for example). In our experience, we found that positive resists worked well with acid gold plating solutions, and have successfully used products manufactured by Technics, Inc., and Transene Company, Inc. After the resist has been stripped, the spacer layer is etched out from under the beams, leaving them freely suspended over the resistor layer and counter electrode.

The I/V characteristics shown in Figure 4 are typical for H-switches with silicon resistors. The nonlinearity of the "on resistance" is expected because the contact between the switch and the silicon is a purely mechanical one. The turnon voltages of the beams we tested were, in general, higher than would be expected from a mathematical model. Close observation showed that the beams tended to curve away from the substrate slightly over their length.

References

- [1] IEEE Transactions on Electron Devices, Vol. Ed. -14, No. 3, March 1967.
- [2] International Electron Devices Meeting, IBM Corp., San Jose, California, pp. 100 - 103, 1978.

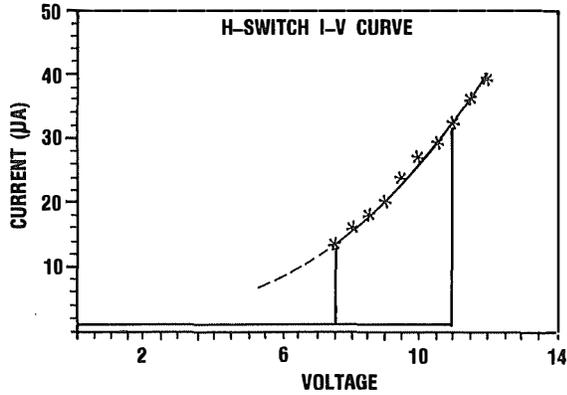


Figure 4