# HIGH-DENSITY SOLID-STATE IMAGE SENSORS

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## Abstract

The most highly developed of solid-state sensors are visible image sensors. Visible image sensor arrays with more than a million picture elements and with noise levels in the tens of electrons have been developed. In this paper the architectures of image sensors are reviewed, and the key issues are discussed. As an example of the present status of sensor technology, results on a 360,000-pixel charge-coupled image sensor are presented.

## Sensor Architectures

The first visible image sensor array was reported in 1967 [1]. However, the development of present-day sensors occurred after the discovery of the charge-coupled device (CCD) in 1970 [2]. The first applications for solid-state sensors were in military and commercial systems. Most of these sensors were linear arrays. More recently, area arrays have been developed for consumer applications. Owing to the continuing development of process technology for silicon integrated circuits, the cost of solid-state imagers is rapidly becoming competitive with the electron-beam-scanned camera tubes such as the saticon. Sensor arrays with 180,000 pixels are in production, and arrays with 360,000 pixels are in advanced development. The advances in silicon VLSI technology that made large-area arrays feasible have also made possible linear arrays with up to 5732 elements [3,4], high-sensitivity time-delay-and-integrate (TDI) scanners [5], very high-frame-rate imaging arrays for high-speed video photography [6], and very high-resolution arrays for astronomy [7].

An image sensor consists of photosensitive elements that convert the incoming light to charge and readout structures that transfer the charge to the output. Three major classes of photosensitive elements are in wide-spread use: the photodiode, the photocapacitor, and the photoconductor. The structure and band diagrams for these photosensitive elements are illustrated in Fig. 1. The photodiode consists of a p-n junction. Usually the implantation for the photodiode is tailored to yield a high electric field from the surface to aid in collection of photoelectrons generated near the surface, giving a high blue sensitivity. Owing to the low capacitance of the diode structure, the charge storage capacity of the photodiode is usually small. For image sensor array applications, the diode is usually fabricated in a p-well to reduce crosstalk and blooming. A variant on the photodiode is the $p^+$-n-p photodiode [8], in which a heavily doped $p^+$ layer is placed near the surface and the n-type layer is lightly doped and is fully depleted during operation. The $p^+n$ front junction results in a factor of 5 or more charge capacity, as compared to the normal photodiode, as well as reduced image lag.

The photocapacitor consists of a thin polysilicon gate above an oxide. Owing to the high optical absorption of the polysilicon, the quantum efficiency is lower than in the photodiode, particularly in the blue. The photocapacitor is used most widely in the form of a frame-transfer CCD or the CID, although photocapactor arrays have been used for very high-speed applications [6]. Owing to the high capacitance of the MOS structure, the photocapacitor has the highest charge of all the photosensitive elements.

Recently, there has been great excitement over the development of photoconductive films such as hydrogenated amorphous silicon (α-Si:H) [9]. These films, deposited on top of an interline or X-Y-addressed diode array, result in a vertical integration of sensors. The α-Si:H photoconductors consist of a back contact (such as aluminum) that contacts the diode in the underlying array, an α-Si:H layer ~1 μm thick, and a transparent top electrode. The photoconductor is biased to complete depletion. Photogenerated carriers are swept out of the photoconductor and stored in the underlying diode. The photoconductor offers high quantum efficiency, very high area utilization, and internal antiblooming.

The major classes of readout architectures for image sensors are the frame-transfer CCD [10,12], the interline-transfer CCD [13-16], and various X-Y-addressed MOS photodiode arrays [6,9,17-20] (Fig. 2). The frame-transfer CCD consists of an illuminated imaging area with vertical registers to integrate and transfer the charge, a storage register to store the charge during readout, and a horizontal transfer register. For television applications both the image and storage areas store one field (242 lines for NTSC television). Vertical interlacing is accomplished by integrating under different electrodes during the two fields, accomplishing a half-pixel shift in the relative position of the pixel. Frame-transfer CCD's have been constructed with two and three levels of polysilicon as well as with one level of polysilicon in virtual-phase CCD's [10]. Since the entire pixel area is photosensitive, the quantum efficiency is very high. However, absorption of blue light in the polysilicon electrodes reduces the blue efficiency. At the end of each field, the integrated charge must be transferred from the image to the storage register. This transfer, which typically requires almost a millisecond, results in some vertical image smearing owing to the very low capacitance of the CCD output (<40 fF); the CCD has very low noise and hence very good low-light-level performance. Output noise values of <50 rms electrons at video rates have been reported.

The interline CCD imager consists of vertical CCD registers used for charge transfer and photodiodes for light sensing and charge storage. For NTSC television there would be 484 diodes vertically and 242 stages of the CCD shift register. At the end of one field the charge from the top diode in each stage is transferred onto the vertical CCD register, while in the other field the charge from the bottom diode is transferred. The vertical registers are optically shielded with aluminum. Owing to the separation of light-sensing and charge-transfer functions, the photodiode typically occupies only 25-40% of the cell area. This results in a lower overall quantum efficiency as compared to the frame-transfer CCD. However, use of photoconductive layers overlying the sensor could greatly reduce this disadvantage.

The unit cell of MOS X-Y-addressed imagers consists of a photodiode (or photocapacitor), a transfer

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gate, and a diffusion contacted by a metal signal line. The transfer gates are addressed by a vertical scan generator, usually a dynamic shift register, which addresses each row sequentially. Horizontal charge readout may be accomplished with horizontal signal lines connected to the vertical signal lines by FET switches controlled by a horizontal scanner. Other X-Y-addressed arrays utilize a CCD for horizontal readout. Owing to the use of a metal signal line instead of a CCD for vertical transfer, the MOS array has a larger fraction of each pixel devoted to the photodiode, resulting in higher quantum efficiency. The MOS array is also simpler to manufacture. However, the sensitivity of the MOS imager at low light levels is severely constrained by the KTC and the pattern noise of the high-capacitance horizontal and vertical signal lines. Although the use of a horizontal CCD reduces the horizontal readout noise, the KTC noise of the vertical signal lines results in a factor of 10 higher noise than the interline CCD readout.

## A 360,000-Pixel Solid-State Image Sensor

### Sensor Design

As an example of the performance of present solid-state sensors, a 360,000-pixel charge-coupled image sensor will be described [11]. The sensor is used for imaging color photographic negatives on television, which places some unique demands on a solid-state sensor. These include wide dynamic range, low pattern noise, high resolution, and excellent color reproduction.

The sensor architecture is shown in Fig. 3a. The sensor consists of a four-phase CCD image area, dual two-phase horizontal registers, and separate output amplifiers for each of the three colors. During the vertical retrace interval the photographic negative is illuminated. The vertical clocks are held constant to integrate the signal charge. At the end of the vertical retrace interval the signal is read out. A row at a time is transferred into the horizontal registers. The charge from columns with green color filters is transferred to the top register, while the charge from the alternate columns with red and blue color filters is transferred to the bottom register. The dual horizontal register design was required to achieve the 12-$\mu$m horizontal column spacing without a third level of polysilicon. The horizontal registers are read out at a 7.15 MHz pixel rate. The charge is sensed by floating diffusion outputs and buffered by dual-stage buried-channel source followers. The use of dual-stage source followers allowed optimization of the first stage for low input capacitance and the second stage for high drive current. The use of the buried-channel FET design reduced low-frequency (1/f) noise.

A photomicrograph of the image sensor is shown in Fig. 3b. The image area is 8.8 mm (H) x 6.6 mm (V). A schematic of the pixel is shown in Fig. 3c. The channel-stop region is 2 $\mu$m wide, and the buried channel is 10 $\mu$m wide. The gate oxide under both the first and second polysilicon electrodes was 1600 Å thick, to maximize optical transmission in the blue. The polysilicon layers were both 1700 Å thick. Source-drain regions were formed by shallow arsenic implantation to minimize short-channel effects in the output structure.

### Spectral Response

In a color image sensor in which the photosensitive area is fully covered by polysilicon, careful choice of the polysilicon thickness is required to achieve adequate transmission in the blue while maintaining sufficiently low resistance to transfer charge vertically. Figure 4a shows the optical absorption coefficient of polysilicon as a function of wavelength. Figure 4b shows the measured spectral response of the sensor along with the response calculated from the known layer thicknesses and the optical constants. At wavelengths below 500 nm the response is dominated by optical absorption in the polysilicon electrodes. Between 500 and 800 nm the response is dominated by structure due to optical interference within the polysilicon and the gate oxide. Beyond 800 nm the light is absorbed well below the silicon surface, and the spectral response decreases, owing to recombination of the photogenerated electrons.

Organic color filter arrays are fabricated on top of the sensor in an R-G-B-G stripe geometry. The color filter arrays are processed by sequential coating, patterning, and dyeing of special photoresists developed for this application. Owing to the narrow (2 $\mu$m) light-shield width, extreme resolution and sharpness requirements are placed on the resist materials. The dyes for this color filter array were specifically designed for imaging photographic negatives.

### Charge Capacity

Because of the large density range of photographic negatives, a wide dynamic range is required in the sensor. There are two limitations to charge capacity in a buried-channel CCD: (1) the interaction between electrons and interface states at the $Si-SiO_2$ surface and (2) the potential difference between well and barrier electrodes. Figure 5a illustrates the first limitation. The electrostatic potential and the electron density are shown as a function of depth for three different quantities of charge in the channel. As more electrons are added to the channel, the barrier to the surface decreases and the electron concentration at the surface increases. Electrons can be captured at interface states when electrons come in contact with the surface.

Owing to the narrow channel width, two-dimensional effects significantly reduce charge capacity. Figure 5b shows the electrostatic potential and electron distribution in two dimensions calculated by finite-difference techniques. The electron distribution is shown at the transition between buried- and surface-channel operation ($\phi_{CH} - \phi_s = 300$ mV) for a $1 \times 10^{12}$ $cm^{-2}$ buried-channel dose. The electrons occupy only the center 4 $\mu$m of the 10-$\mu$m channel. For a $2 \times 10^{12}$ $cm^{-2}$ buried-channel dose with a significantly larger barrier between channel and surface, the electrons occupy the center 7 $\mu$m of the 10-$\mu$m channel. The barrier between the electrons in the channel calculated as a function of the electron density is shown in Fig. 5c for two buried-channel doses using one- and two-dimensional models. Figure 6 shows the experimentally measured differential charge-transfer inefficiency for the image area as a function of the number of electrons per pixel for the two buried-channel doses. The $1 \times 10^{12}$ $cm^2$ dose yields a capacity of 100,000 electrons per pixel, and the $2 \times 10^{12}$ $cm^2$ dose 800,000 electrons, in good agreement with the two-dimensional model.

### Noise

The noise sources in this sensor include pattern and shot noise from dark current, output amplifier noise, and photosensitivity pattern noise due to the sensor and the color filter array.

The dark current in better sensors at room temperature was 5 nA/cm$^2$ or 1600 electrons per pixel. Measurements of the dark current in test structures adjacent to the sensor as a function of gate voltage showed that surface generation accounted for 2.5 nA/cm$^2$, generation in the buried-channel implanted region for 1 nA/cm$^2$, generation in the unimplanted portion of the depletion layer for 0.5 nA/cm$^2$, and diffusion current for 0.1 nA/cm$^2$. Comparison of test structures with and without channel stops indicated that the channel stops contributed an additional 1 nA/cm$^2$ to the overall dark current. Subsequent analysis by transmission electron microscopy revealed dislocation loops 100 Å in diameter in the implanted region of the channel and precipitates 50 Å in diameter in the channel-stop regions.

The largest random noise source is the output amplifier at 200 rms electrons per pixel in a 3.5-MHz bandwidth. The output amplifiers are two-stage buried-channel source followers with sensitivity of 2 μV/electron. Owing to the use of buried-channel transistors in the source follower and to double correlated sampling in the signal processing, the output amplifier noise is almost entirely a result of thermal noise in these transistors.

In Fig. 7 the signal and the noise from various sources are plotted as a function of the density of the photographic negative. The largest noise source is the output amplifier noise at 200 rms electrons per pixel. The dynamic range of the sensor is 70 dB. This exceeds the dynamic range required for imaging photographic negatives.

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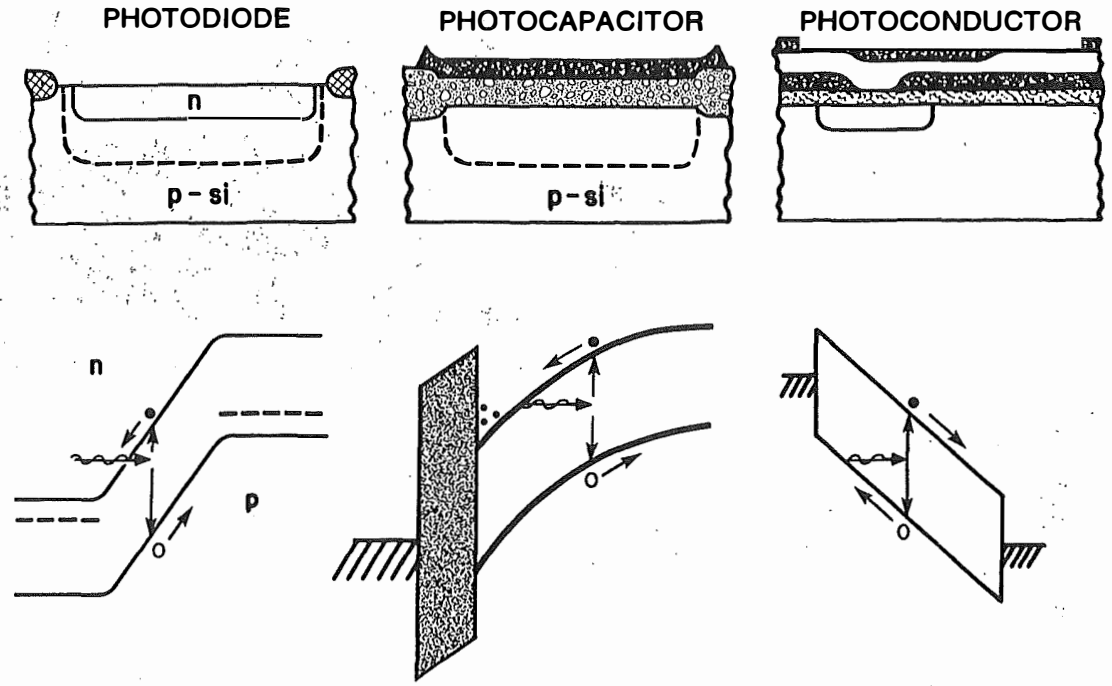



Fig. 1 Cross-sections and band diagrams of photosensitive elements: (a) photodiode, (b) photocapacitor, (c) photoconductor

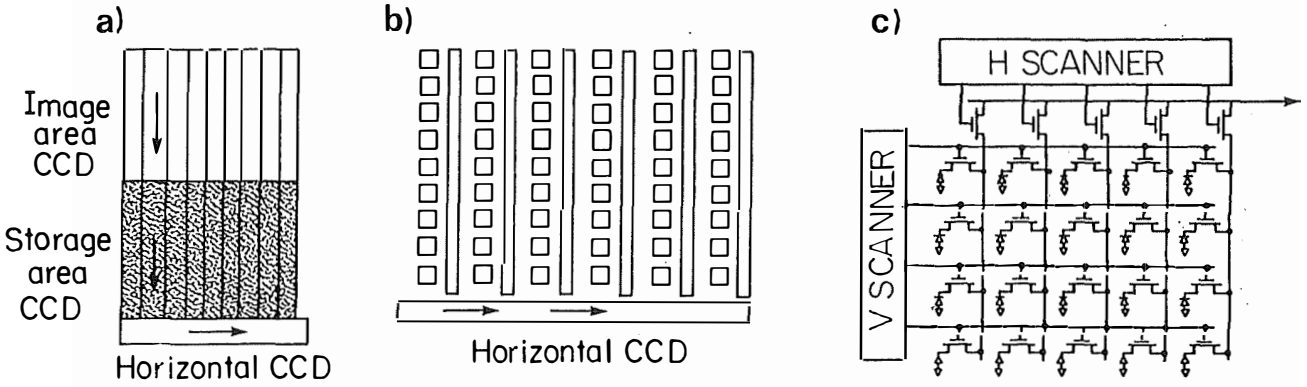
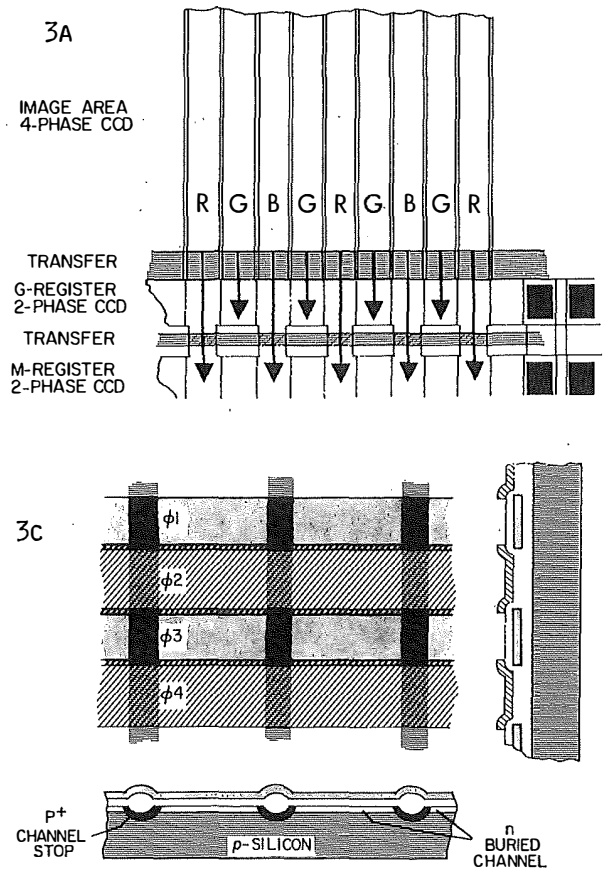



Fig. 2 Architectures of major sensor designs: (a) frame-transfer CCD, (b) interline-transfer CCD, (c) MOS diode array



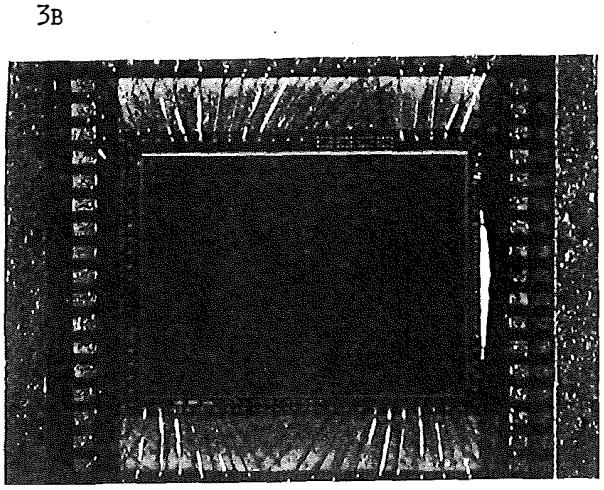
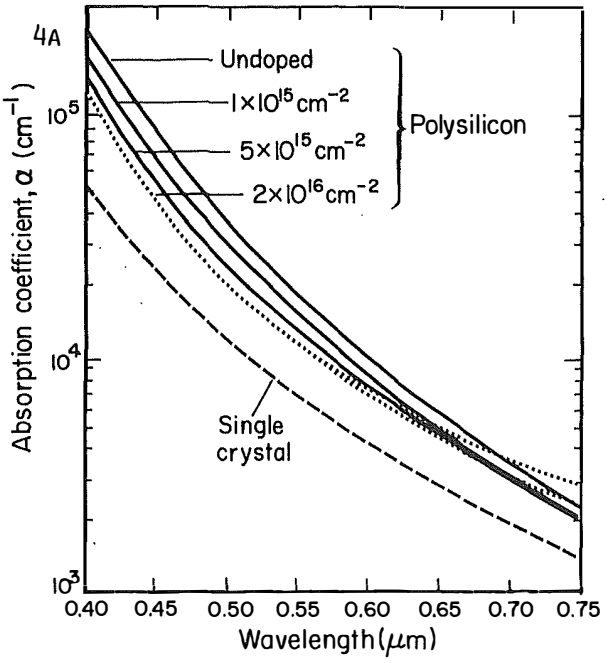




Fig. 3. (a) Design of image sensor. Sensor has 740 columns horizontally with R-G-B-G stripe color filter pattern. Vertical registers are four-phase C.C.D.'s; horizontal registers are two-phase.

(b) Photograph of sensor chip. Image area is 8.8 mm (H) x 6.6 mm (V).

(c) Design of image area. Width of column is 12 $\mu$m, including 2 $\mu$m channel stops.



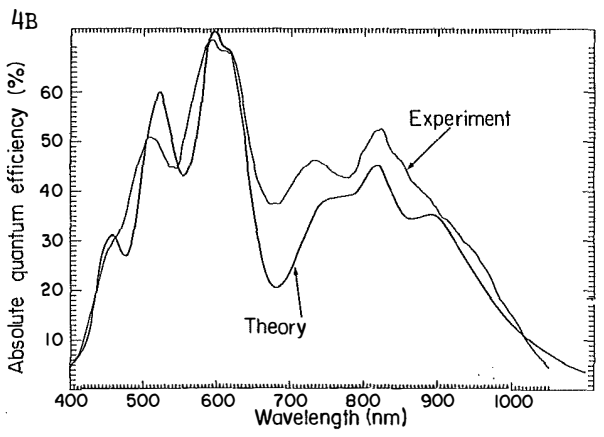
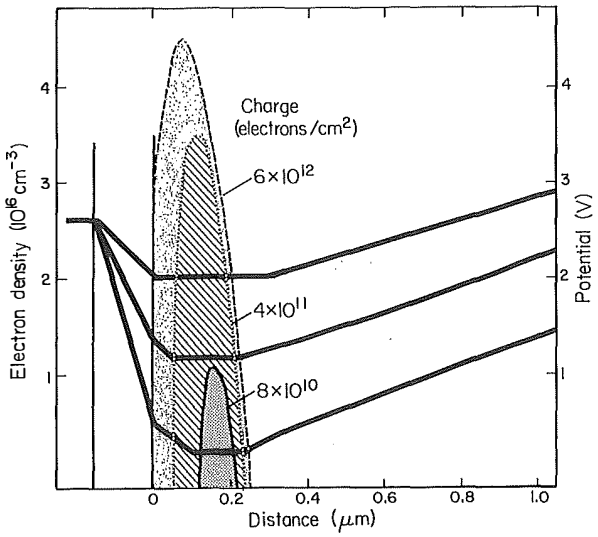




Fig. 4. (a) Absorption coefficient of polysilicon phosphorus doped at various concentrations.

(b) Measured and calculated spectral response of sensor.

5A

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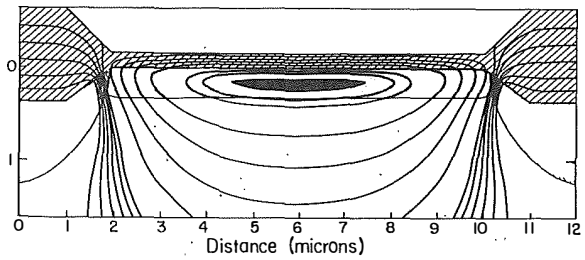


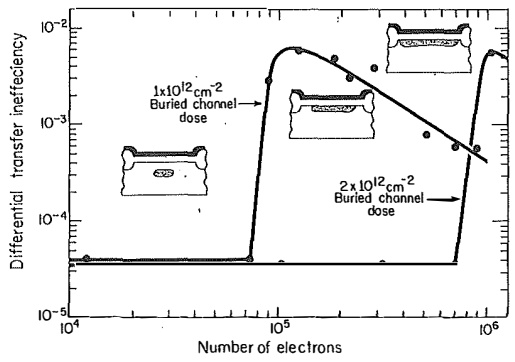


Fig. 6. Differential transfer inefficiency vs. number of electrons per pixel for vertical C.C.D. registers for two buried-channel doses.

5c

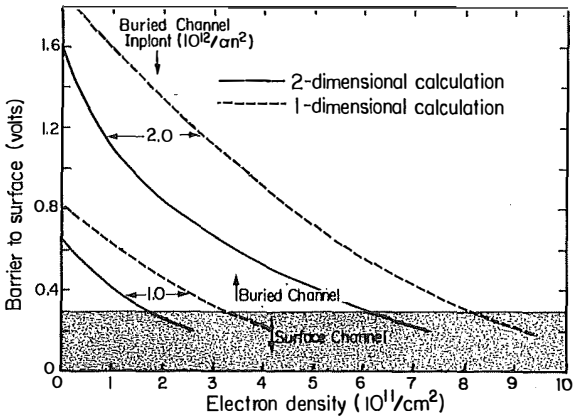


Fig. 5. (a) Electrostatic potential and electron distribution for different quantities of charge in the buried channel.

(b) Electrostatic potential and electron distribution in two dimensions for 10 $\mu$m wide buried channel.

(c) Potential barrier between buried channel and surface as a function of electron concentration for two buried-channel doses. Results of one- and two-dimensional models are shown.

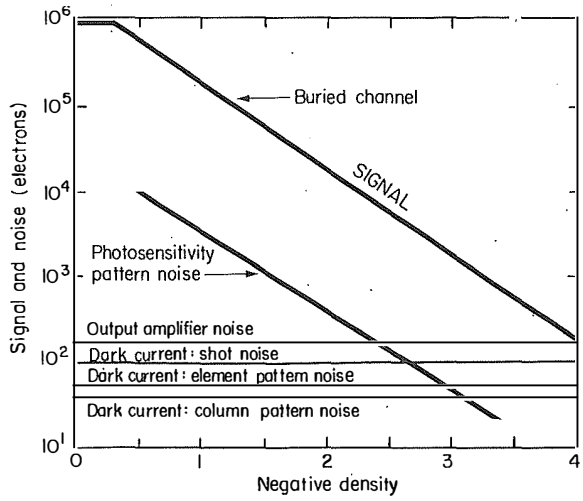


Fig. 7. Signal and noise as a function of the density of the photographic negative. Dynamic range of the sensor is 70 dB.